USB2.0 macro

Design of printed circuit boards

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Fujitsu Limited
1. Preface

To satisfy the characteristics of USB2.0 PHY and pass the compliance test, instructions on the design of printed circuit boards are provided. Follow these instructions when designing a board, and check the system operation.

Figure 1 shows the schematic diagram. The USB2.0 PHY has the HSDPPAD and HSDMPAD pins conducting High Speed Mode signal transactions; the FSDPPAD and FSDMPAD pins conducting Full Speed Mode signal transactions and are used to configure termination resistance; the EXT12K pin to generate the reference voltage; the CRYCLK48 clock input pin; and several analog power supply pins and ground pins.

For the USB2.0 PHY, external resistors must be connected outside of the chip. These resistors should be placed as close to the pins as possible. If the resistors are not close to the pins, jitter and overshoot/undershoot will be generated in the output waveform.
Figure 1  USB2.0 PHY analog pins and externally connected circuits
2. D+/D-

- For the D+/D-, as USB2.0 PHY, the HSDPPAD and FSDPPAD pins, and the HSDMPAD and FSDMPAD pins are combined respectively.

- Place the resistors (external 39Ω) close to the LSI’s pins. If not close, the output waveform will have overshoot/undershoot or greater jitters. Keep the distance between the resistors and the pins up to 5 [mm].

- The dumping resistors are not essential. However, if overshoot/undershoot occurs in the waveform due to uncertain causes, insertion of dumping resistors could solve the problems. When designing the printed circuit board, consider insertion of the dumping resistors. The resistors should have resistance of about 20[Ω].

- Though it depends on case, the precision of the dumping resistors should be ±1%.

- Shorten the wire lengths between the pins and the joints as much as possible. In this case, the HSDP (DM) should be the shortest.

- Shorten the D+ and D- wire lengths to the cable connectors as much as possible. In the USB Specifications, it is required that the signal propagation time between the LSI pins and the connectors be limited up to 1 [ns] for the upstream of the function and up to 3 [ns] for the downstream of the host.

- Based on the USB Specifications, the impedances of the wires on the board must be matched. The impedance characteristics should be as follows.

Impedance characteristics:
- Differential impedance (Zdiff): 90Ω ±10% @240MHz
- Characteristics impedance (Z0): 45Ω ±10% @240MHz
2. D+/D- (continued from the previous page)

j. Wire adjacently the HSDP and HSDM; the FSDP and FSDM; and the D+ and D-. The wiring pitch and wire width through the adjacent wires must be constant.

k. The HSDP and HSDM; the FSDP and FSDM; and the D+ and D- must not be bent 90°. When bending is needed, bend them up to 45°. If 90° bending is required, use 45° bending twice instead. Reducing the bending degree is preferable for the characteristics.

l. Assign a ground on either side of a pair of the HSDP and HSDM; the FSDP and FSDM; and the D+ and D- for shielding. For the shielding, the space for at least the width of the signal wires must be provided.

m. Do not allow wires of other signals on upper and lower layers to cross the wirings of HSDP and HSDM, and FSDP and FSDM.

n. On the layer just below D+/D-, provide a ground plain. Extend the ground plain rightwards and leftwards so that it is about the same size as the shielding on the upper layer. Avoid generation of vertical slits on the ground.

o. Use the same power supply for the grounds explained in l and n.

p. Use the uppermost layer for the D+/D- wiring.

q. Avoid using VIAs. They cause reflection.

r. The effectiveness of common mode choke filters depends on external conditions. The printed circuit board should be designed in such a way that common mode choke filters can be inserted later.
3. EXT12K

a. Wire the EXT12K pin to the ground (AVSB) via an external resistor of 12K[ohm].

b. Place the external resistor of 12K[ohm] as close to the EXT12K pin as possible to make the wiring between them shorter.

c. The precision of the external resistor of 12K[ohm] must be 12KΩ ±1%.

d. The EXT12K is used for the reference voltage within the USB2.0 PHY macro. Propagation of crosstalk to this pin affects the entire USB operation. Do not allow wiring of other signals to cross or goes adjacently to the wiring between the EXT12K pin and external resistor of 12K[ohm]. Even power supply and ground wirings, if they are of more than one type, cannot cross the wiring.

e. To shut off noise from other signal lines, the EXT12K may be shielded by the grounds surrounding the EXT12K as shown in Figure 5.

f. Keep the capacitance added to the EXT12K up to 20[pF] including the wiring parasitic capacitance of the board and package.

g. Keep the peak-to-peak noise amount of KEXT12K pin up to 50[mV].

h. The noise of EXT12K pin is measured as follows:
   - Measurement position: Between the EXT12K pin and GND(AVSF1) pin or near the ends of the external resistor of 12K[Ω]
   - Probe: Input resistance ≥ 1[MΩ]
   - Input capacitance ≤ 1[pF]
   - Band ≥ 1.5[GHz]
4. Power supply and ground

- Noise generated in an analog power supply (AVDF1, AVDF2, AVDB, AVDP) or analog ground (AVSF1, AVSF2, AVSB, AVSP) affects the operation and characteristics of the USB2.0 macro. Separate them from digital power supply and ground.

- Provide larger area for the power supply and ground pattern as possible.

- As shown in Figure 6, insert filters for each power supply pin. For the grounds, insert filters to separate them from digital grounds. Share the grounds within the macro.

- The USB2.0 macro’s analog power supplies and grounds cannot be used by other devices.

- Do not allow the wires of signals with frequent signal transitions to cross analog power supply and ground wirings above or below the analog power supply and ground wirings.

- Keep the voltage fluctuation of analog power supply and ground up to 30mV.

- As a countermeasure against noise (such as switching noise and crosstalk), reinforce the power supply and ground by inserting bypass capacitors.

Figure 6  Power supply and ground wiring
5. **Bypass capacitor**

   a. Take effective measure against noise by using bypass capacitors.

   b. Place the bypass capacitors as close to the LSI as possible.

6. **48[MHz] reference clock**

   a. Keep the precision of 48[MHz] reference clock up to 100 ppm, and the jitter up to 100 ps.

   b. Influence (such as crosstalk noise) of other signal wires on the reference clock causes jitters and affects operation. As countermeasures, provide enough space from other signal lines on the printed circuit board, or shield the clock with stable power supply wires.

   c. When inputting the reference clock from an oscillating module, it is possible that the clock waveform is deformed and the USB macro’s characteristics are degraded. To enable prompt countermeasure in that case, such a pattern that dumping resistors can be inserted between the oscillating module and the input pin of the reference clock should be designed.