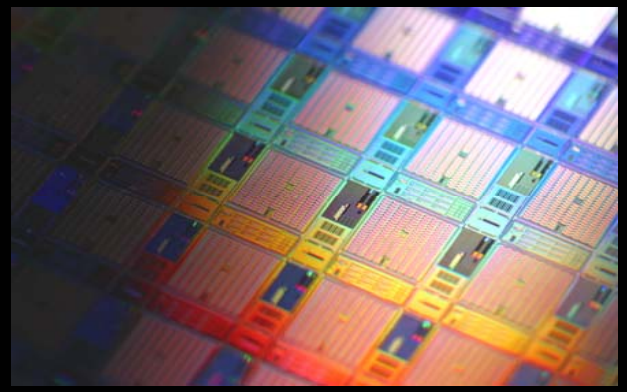


FUJITSU

Display Timing Calculation

(MB86R01 'Jade')

Display Timing Formulae

$f_{dot\_clk} = pixel\ clock$

$f_v = vertical\ \ frequency$

$f_{ref} = reference\ clock\ (PLL)$

$SC = Scaler$

$f_h = horizontal\ \ frequency$

$$f_{dot\_clk} = f_v * VTR * HTP$$

$$f_{dot\_clk} = \frac{f_{ref}}{SC}$$

$$f_v = \frac{f_{dot\_clk}}{VTR * HTP}$$

$$f_h = V_t * VDP$$

$$JADE : f_{ref} = 666Mhz$$

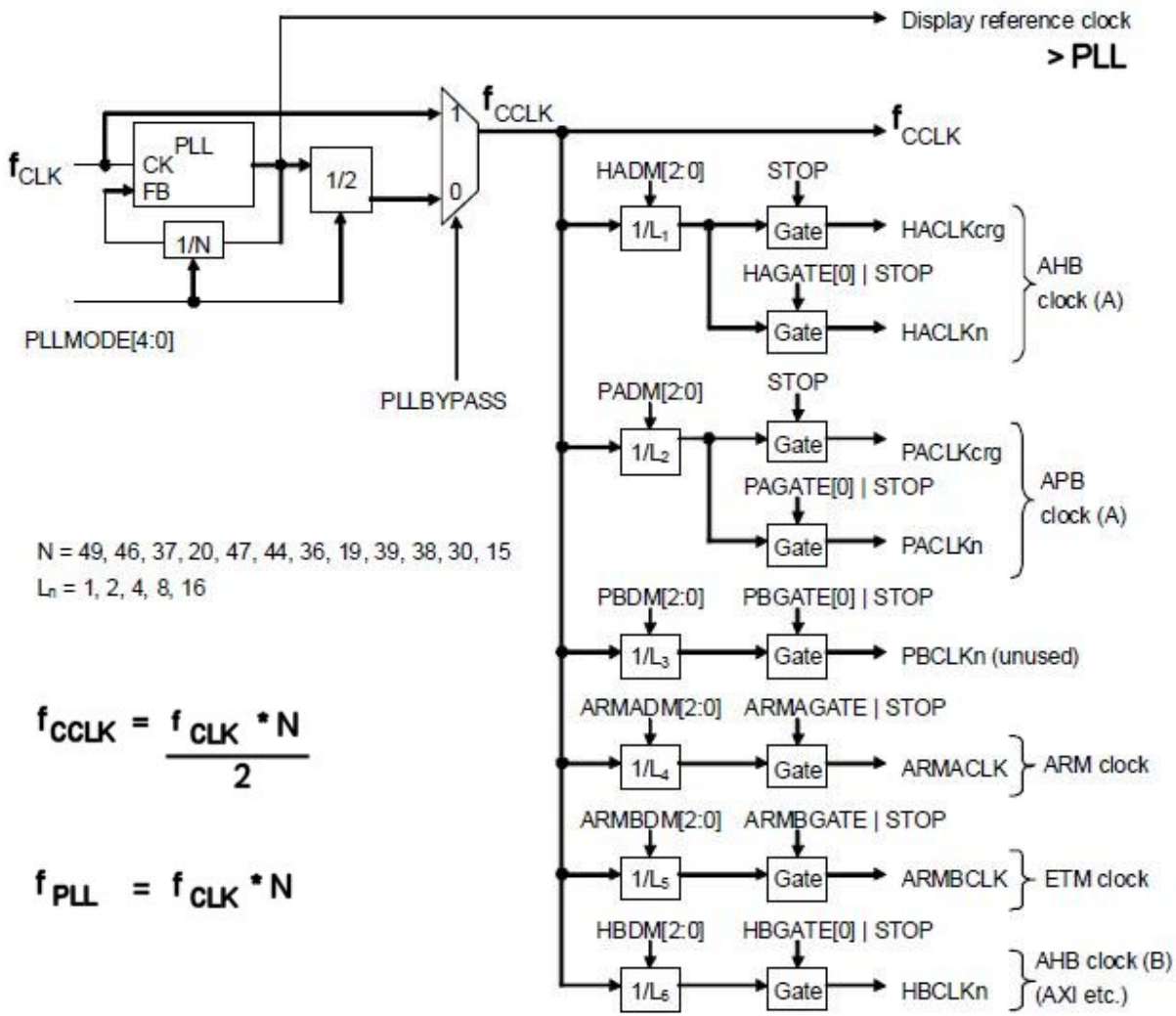
$$f_v = \frac{f_{ref}}{SC * VTR * HTP}$$

Note:

$$JADE : f_{dot\_clock} < 67Mhz$$

$$SC = \frac{f_{ref}}{f_v * VTR * HTP} = \frac{f_{ref}}{f_{dot\_clk}}$$

Clock Generation in Jade



N = 49, 46, 37, 20, 47, 44, 36, 19, 39, 38, 30, 15

L_n = 1, 2, 4, 8, 16

$$f_{CCLK} = \frac{f_{CLK} * N}{2}$$

$$f_{PLL} = f_{CLK} * N$$

Display Timing Parameters

HTP	Horizontal Total Pixels	**VTR**	Vertical Total Raster
HSP	Horizontal Synchronize pulse Position	**VSP**	Vertical Synchronize pulse Position
HSW	Horizontal Synchronize pulse Width	**VSW**	Vertical Synchronize pulse Width
HDP	Horizontal Display Period	**VDP**	Vertical Display Period

Display Timing Guideline - 1

1. **Select the display parameters from the display panel specification**

   0 < HDB ≤ HDP < HSP < HSP + HSW + 1 < HTP
   0 < VDP < VSP < VSP + VSW + 1 < VTR

Note:
Skew occurs between the syncs and the RGB/DE signals (the RGB and DE signals are delayed) :
- Coral family – 13 pixel clock cycles
- Carmine – 15 pixel clock cycles
- The timing at the GDC pads is different to the register settings
- Panels requiring less H-sync back porch are not supported – the H-sync has to be delayed by external logic

2. **Calculate the pixel frequency**

$$f_{dot\_clk} = f_v * VTR * HTP$$

3. **Calculate the scaler value**

$$SC = \frac{f_{ref}}{f_v * VTR * HTP} = \frac{f_{ref}}{f_{dot\_clk}}$$

Select integer value:
->Round down
->Round up

Calculate the resulting pixel vertical frequency with the selected scaler value:

$$f_{dot\_clk} = \frac{f_{ref}}{SC} \qquad f_v = \frac{f_{ref}}{SC * VTR * HTP}$$

$$f_{dot\_clock} < 67\,Mhz$$

Check that the calculated values fulfill the display specifications.
Optional: adapt the blanking area to reach a more precise result.

Display Timing Guideline - 2

4. Set scaler register value

The scaler value depends on the selected offset

Divides display reference clock by the preset ratio to generate dot clock

Offset = 0		Offset = 100_H	
x00000	Frequency not divided	000000	Frequency not divided
x00001	Frequency division rate = 1/4	000001	Frequency division rate = 1/2
x00010	Frequency division rate = 1/6	000010	Frequency division rate = 1/3
X00011	Frequency division rate = 1/8	000011	Frequency division rate = 1/4
:		:	
x11111	Frequency division rate = 1/64	111111	Frequency division rate = 1/64

When n is set, with Offset = 0, the frequency division rate is 1/(2n + 2).

When m is set, with Offset = 100h, the frequency division rate is 1/(m + 1).

Basically, these are setting parameters with the same function (2n + 2 = m + 1). Because of this, m = 2n + 1 is established. When n is set to the SC field with Offset = 0, 2n + 1 is reflected with Offset = 100h.

Also, when PLL is selected as the reference clock, frequency division rates 1/1 to 1/5 are non-functional even when set; other frequency division rates are assigned.

16.7.7.2. Display controller registers

Base = DisplayBase0(=0xF1FD_0000) or
Base = DisplayBase1(=0xF1FD_2000) = DisplayBase0+0x2000

Offset	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000	DCM0 (Display Control Mode 0)																															
	DEN												L45E	L23E	L1E	L0E	CKS	LCS		SC					EEQ	EDE	EOF	EOD	SF	ESY	SYNC	
100	DCM1 (Display Control Mode 1)																															
	DEN										L5E	L4E	L3E	L2E	L1E	L0E	CKS	LCS		SC					EEQ	EDE	EOF	EOD	SF	ESY	SYNC	
104	DCM2 (Display Control Mode 2)																															
																												RUM1			RUF	RUM0
108	DCM3 (Display Control Mode 3)																															
							GVD	VPWMs	Gswap	CSYz	RGBrv	RGBsh		BSYe	MBST							POM	CKdtr	CKinv	CKDe			CKDn				
004	HTP (H Total Pixels)																				HDP (H Display Period)											
008	HDB (H Display Boundary)																															
00C	VSWH	VSW							HSW												HSP (H Sync pulse Position)											
010	VTR (V Total Rasters)																															
014	VDP (V Display Period)																				VSP (V Sync pulse Position)											
018	WY (Window Y)																				WX (Window X)											
01C	WH (Window Height)																				WW (Window Width)											

NOTE:
Also, when the PLL is selected as the reference clock, frequency division ratios 1/1 to 1/5 are non-functional even if set (!) other frequency division ratios are assigned.

Therefore – valid setting range: 1/6 ... 1/64

NOTE:
To achieve timings that require a setting higher than 1/64, the LCS bit of the DCM0/1 register can be used:

LCS = 0: $f_{dot\_clk} = (f_{PLL})/SC$

LCS = **1**: $f_{dot\_clk} = [(f_{PLL})/SC]$***/4***

Display Timing Example - 1

Display Panel:
Toshiba Matsushita Display Technology, LTA065B0D0F (6")
Vertical frequency: 60 Hz

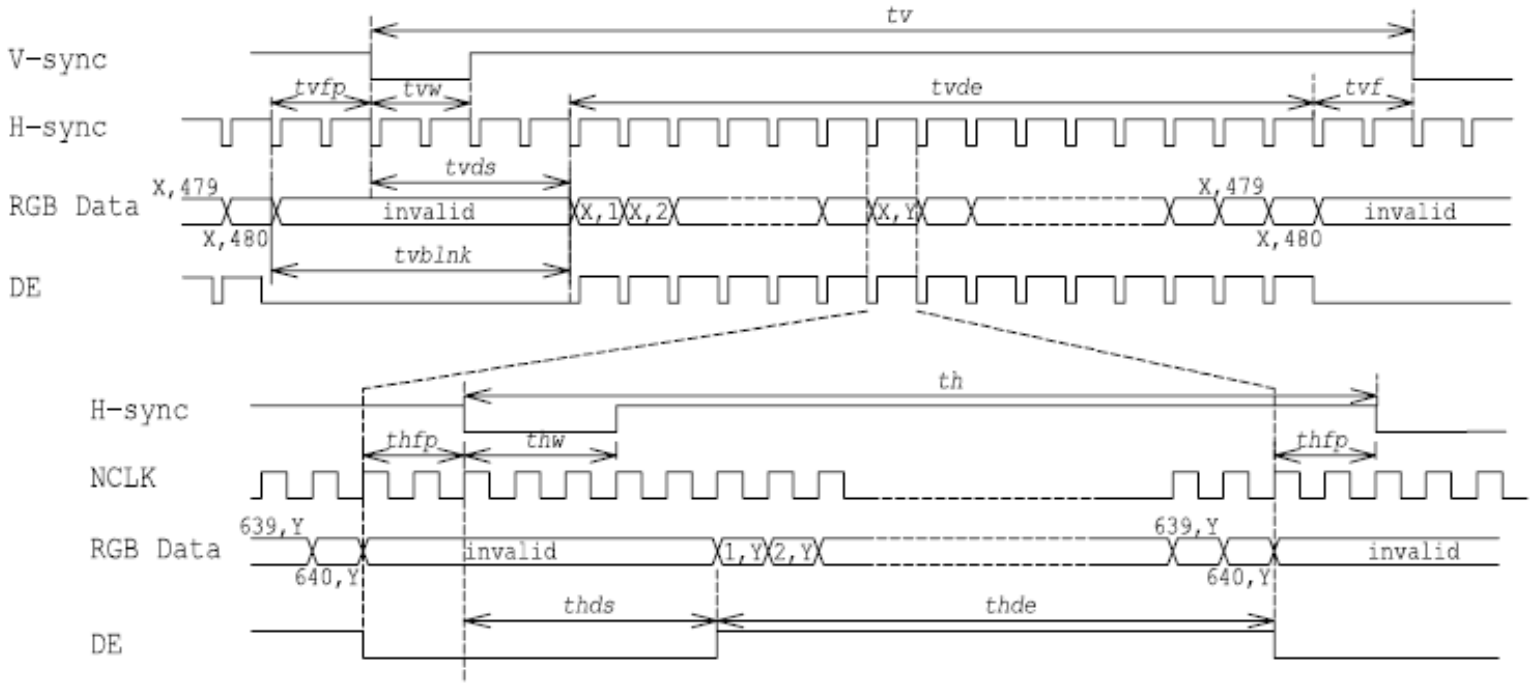
Excerpt from the display specification:

TIMING SPECIFICATION [1) 2) 3) 4) 5)]

<H-Sync/V-Sync+DE Mode>

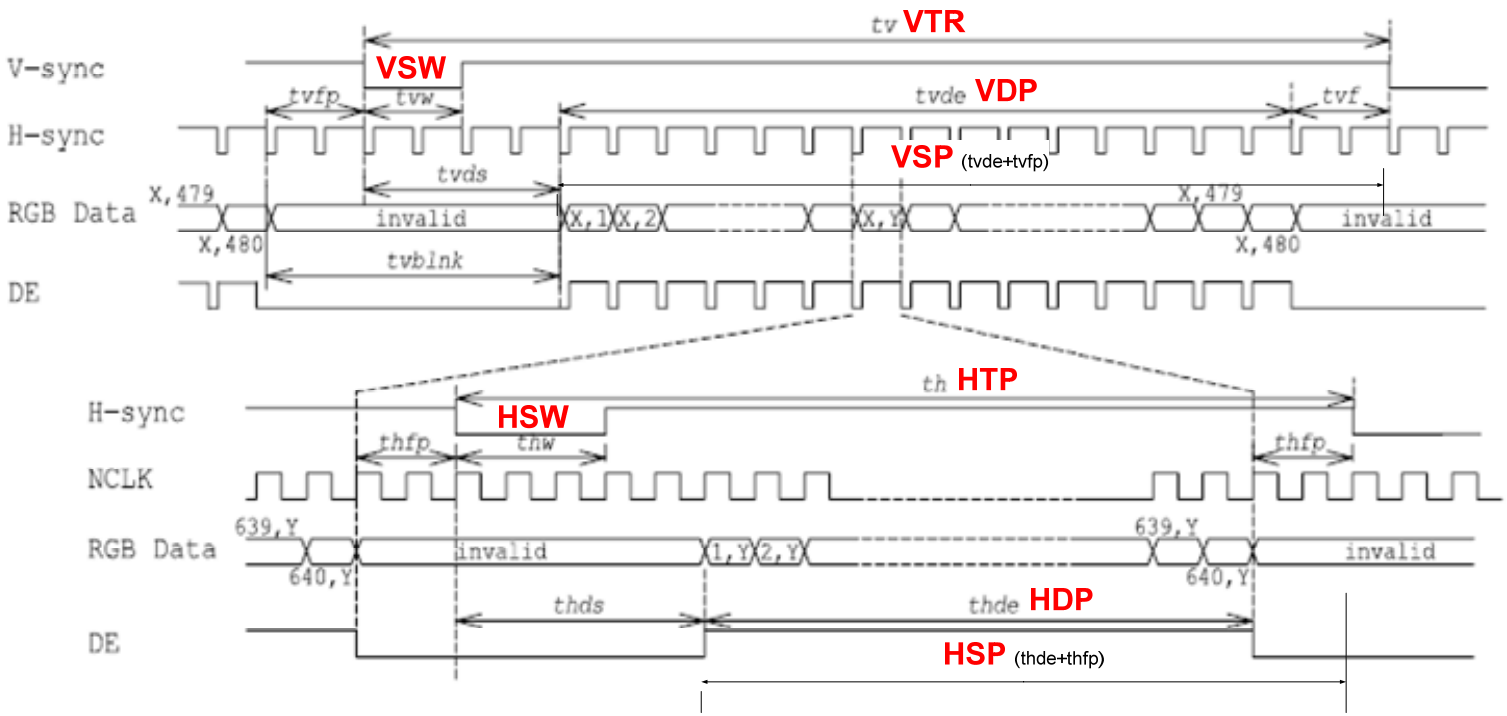
Item	Symbol	min.	typ.	Max.	unit
Frame Period	*tv*	500 ---	525 16.67	550 17.85	*th* ms
Vertical blanking Term	*tvblnk*	20	45	70	*th*
V-sync Pulse Width	*tvw*	2	---	---	*th*
Vertical Front Porch	*tvfp*	2	---	---	*th*
Vertical Data Sync Period	*tvds*	6	---	---	*th*
Vertical Display Term	*tvde*	480	480	480	*th*
Horizontal Period	*th*	740 31.5	800 31.75	860 ---	*tc* us
H-sync Pulse Width	*thw*	8	160	---	*tc*
Horizontal Front Porch	*thfp*	8	---	---	*tc*
Horizontal Data Sync Period	*thds*	8	---	---	*tc*
Horizontal Display Term	*thde*	640	640	640	*tc*
Clock Period	*tc*	35.0	39.7	---	ns
Clock “L” Time	*tcl*	10.0	---	---	ns
Clock “H” Time	*tch*	10.0	---	---	ns
Data Setup Time	*tds*	5.0	---	---	ns
Data Hold Time	*tdh*	10.0	---	---	ns

Display Timing Example - 2



Display Timing Example - 3

1. Select the display parameter



HTP	800	**VTR**	525
HSP	648	**VSP**	482
HSW	160	**VSW**	2
HDP	640	**VDP**	480

$$f_{dot\_clk\max} = clock\,period = t_{c\min} = 35ns = 28.75Mhz$$

$$f_{v\min} = Frame\,Period = tv_{\max} = 17.85ms = 56Hz$$

Display Timing Example - 4

2. Calculate the pixel frequency

$$f_{dot\_clk} = f_v * VTR * HTP = 60Hz * 525 * 800 = 25.2Mhz$$

$$f_{dot\_clock} < 67Mhz$$

3. Calculate the scaler

$$SC = \frac{f_{ref}}{f_v * VTR * HTP} = \frac{f_{ref}}{f_{dot\_clk}} = \frac{666Mhz}{25.2Mhz} = 26.4$$

Round down: SC = 26

$$f_{dot\_clk} = \frac{f_{ref}}{SC} = \frac{666Mhz}{26} = 26.62Mhz -> OK$$

$$f_v = \frac{f_{ref}}{SC * VTR * HTP} = \frac{666Mhz}{26 * 525 * 800} = 60.99Hz -> OK$$

Display Timing Example - 5

Round up: SC = 27

$$f_{dot\_clk} = \frac{f_{ref}}{SC} = \frac{666Mhz}{27} = 24.67Mhz -> OK$$

$$f_v = \frac{f_{ref}}{SC * VTR * HTP} = \frac{666Mhz}{27 * 525 * 800} = 58.73Hz -> OK$$

Try to reach a precise result by modifiying the blanking area:

HTP	860	**VTR**	500
HSP	648	**VSP**	482
HSW	160	**VSW**	2
HDP	640	**VDP**	480

$SC : 26$

$f_{dot\_clk} = 26.4Mhz$

$f_v = 59.57Hz$

4. Set scaler register value

Offset 0x100 -> m = SC-1 = 25 = 0x19
Write register DCM1: 0x1900

THE POSSIBILITIES ARE INFINITE