

MB86297A 'Carminé' Timing Analysis of the DDR Interface

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History

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0 Abstract

This document describes the timing analysis required to ensure proper operation of the DDR interface of the MB86297A 'Carmine' graphics driver from Fujitsu.

1 References

Referenced documents:

- CHWRM Fujitsu, MB86297A 'Carmine' Hardware Reference Manual
rev. 1.22, 25 June 2007
- JESD79E JEDEC Standard, Double Data Rate (DDR) SDRAM Specification
Release E, May 2005
<http://www.jedec.org>

Additional information:

- CIBIS Fujitsu, MB86297A 'Carmine' IBIS Model
rev. 1.7
- CPDG Fujitsu, MB86297A 'Carmine' PCB Design Guideline
rev. 1.30, 4 June 2007
- IBIS IBIS (I/O Buffer Information Specification)
Version 4.2, Ratified June 2, 2006
<http://www.eigroup.org>

All Fujitsu documents listed above are available on the Fujitsu Graphics Solutions website:

<http://www.fujitsu.com/emea/services/microelectronics/displaycontrollers/>

2 Definitions

2.1 Naming Conventions

In order to distinguish between the different timing parameters, the following notation is used:

**_DDR* DDR SDRAM timing parameter, e.g. $t_{DQ\text{SCK_}DDR}$.

The corresponding timing parameter in JESD79E is defined without the suffix.

**_PCB* Timing parameter derived from IBIS simulation of PCB, e.g. t_{CK_PCB}

Timing parameters without any of these suffixes are taken from the CHWRM.

Additionally, minimum and maximum ratings are denoted by **_MIN* and **_MAX* suffixes.

3 Timing Analysis

3.1 Timing Groups

In order to simplify the timing analysis, the DDR signals have been divided into groups with similar timing characteristics. This allows the timing analysis to be done on the timing groups instead of the individual signals.

Figure 1 shows the timing groups in a simplified circuit diagram. Table 1 lists which signals belong to which timing group.

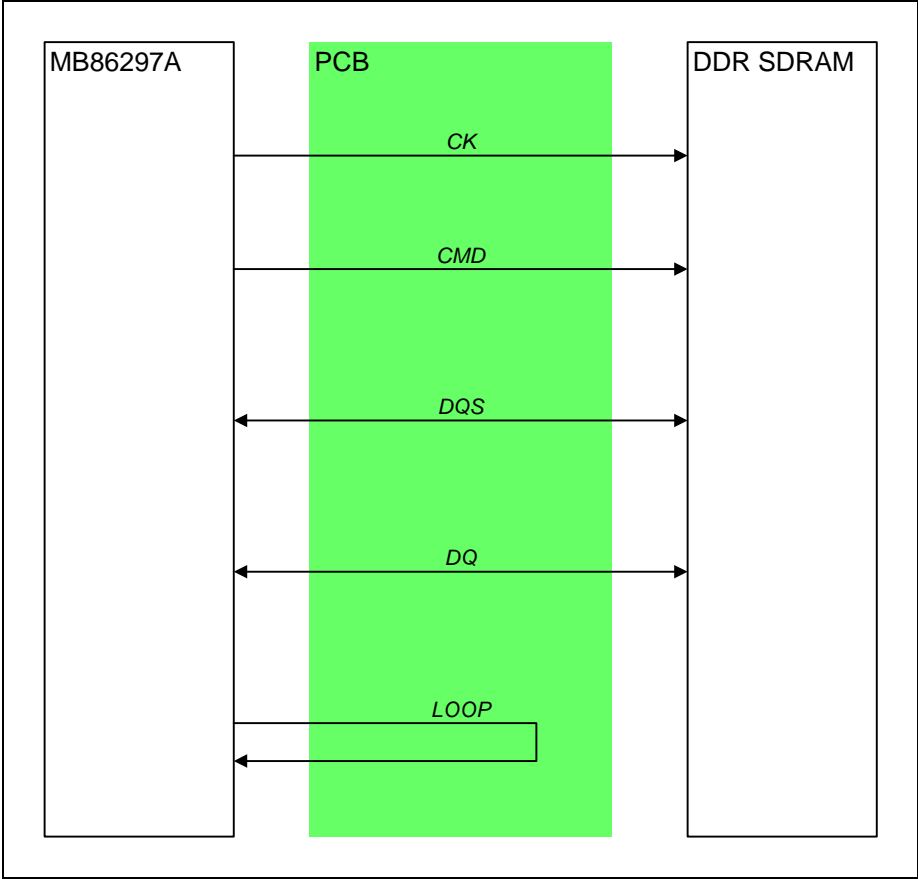


Figure 1 Simplified MB86297A to DDR circuit diagram

Timing Group	Signals	Comment
CK	CK, CK _n	
CMD	CKE, RAS, CAS, WE, A, BA0, BA1	A refers to all address signals
DQS	DQS	
DQ	DQ, DM	DQ and DM refer to all data and data mask signals
LOOP	LOOP	PCB delay compensation loop of MB86297A. This signal is not part of JESD79E.

Table 1 Timing Groups

3.2 PCB Delays

Due to the high speed nature of the DDR interface, the PCB delays have to be taken into account during the timing analysis. Figure 2 defines the PCB delays used throughout this document.

Since it is normally not possible to measure the PCB delays in actual hardware, these parameters have to be derived from IBIS simulations. This also has the added advantage of allowing the timing to be checked before any PCB is produced.

Since the *DQS* and *DQ* groups are bidirectional and the two chips have different pad characteristics, the PCB delays have to be derived for both directions.

Fujitsu provides an IBIS model for the MB86297A. The DDR SDRAM manufacturer should provide IBIS models for their products.

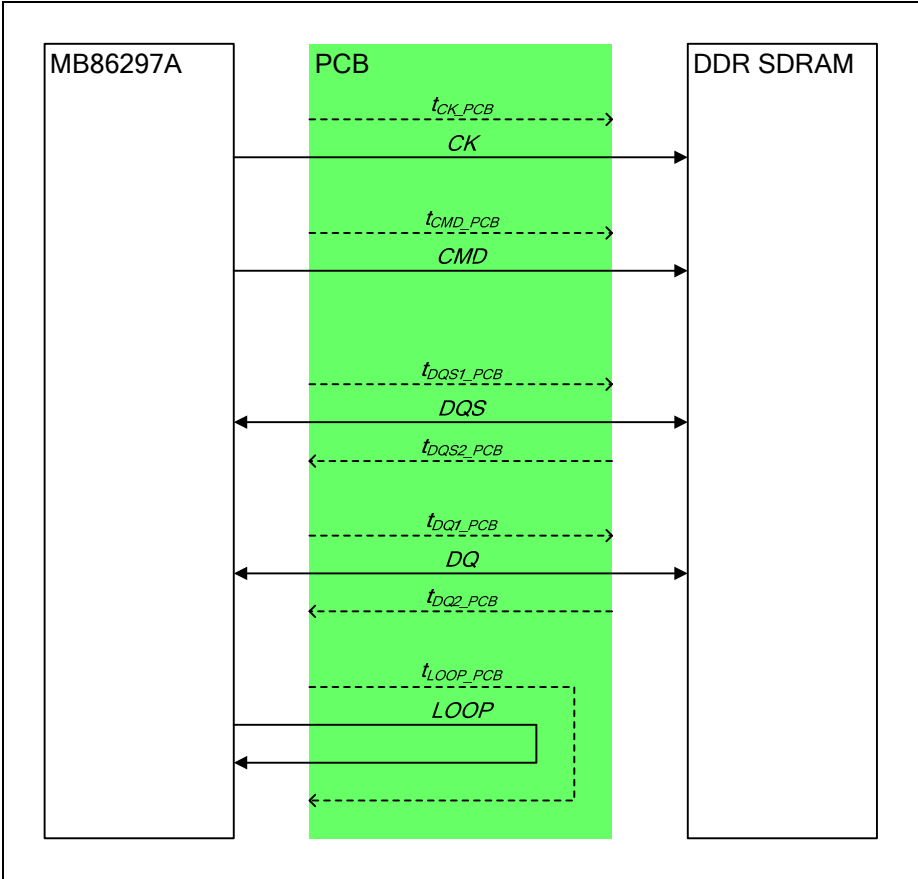


Figure 2 PCB Delays

3.3 Write Timing

In order to achieve timing closure for write operations, all signals have to arrive at the DDR SDRAM within the specified timing conditions.

Skew introduced by the PCB has to be taken into account. For a well balanced design where all the PCB delays are matched, the PCB skew is negligible compared to the available timing margins. If so, the PCB skew can be disregarded. For clarity, the PCB skews have been written within parentheses in the conditions below.

CMD-CK setup and hold timing:

$$(1) \quad t_{VD_setup_CMD} - (t_{CMD_PCB} - t_{CK_PCB}) > t_{IS_DDR_MIN}$$

$$(2) \quad t_{VD_hold_CMD} + (t_{CMD_PCB} - t_{CK_PCB}) > t_{IH_DDR_MIN}$$

DQS-CK setup and hold timing:

$$(3) \quad t_{Skew_DQS_CK_MIN} + (t_{DQS1_PCB} - t_{CK_PCB}) + t_{CK} > t_{DQSS_DDR_MIN}$$

$$(4) \quad t_{Skew_DQS_CK_MAX} + (t_{DQS1_PCB} - t_{CK_PCB}) + t_{CK} < t_{DQSS_DDR_MAX}$$

In the CHWRM, the setup and hold timing is defined as skew between *DQS* and *CK* instead of setup and hold timing. In order to translate these parameters into JESD79E conformant ones, a clock period (t_{CK}) has to be added, as seen in (3) and (4).

DQ-DQS setup and hold timing:

$$(5) \quad t_{VD_setup_DQ} - (t_{DQ1_PCB} - t_{DQS1_PCB}) > t_{DS_DDR_MIN}$$

$$(6) \quad t_{VD_hold_DQ} + (t_{DQ1_PCB} - t_{DQS1_PCB}) > t_{DH_DDR_MIN}$$

3.4 Read Timing

In order to achieve timing closure for read operations, all signals have to arrive at the MB86297A 'Carminie' within the specified timing conditions.

DQ-DQS setup and hold timing:

$$(7) \quad t_{DQSQ_DDR_MAX} + (t_{DQ2_PCB} - t_{DQS2_PCB}) < -t_{SETUP_DQ}$$

$$(8) \quad t_{QH_DDR_MIN} + (t_{DQ2_PCB} - t_{DQS2_PCB}) > t_{HOLD_DQ}$$

Due to the definition of t_{SETUP_DQ} in the CHWRM, the negative value has to be used, as seen in (7).

As for the write timing, the PCB skew of (7) and (8) can be disregarded if the PCB delays of *DQ* and *DQS* are well matched. For clarity, the PCB skews have been written within parentheses in the above conditions.

DQS round trip time:

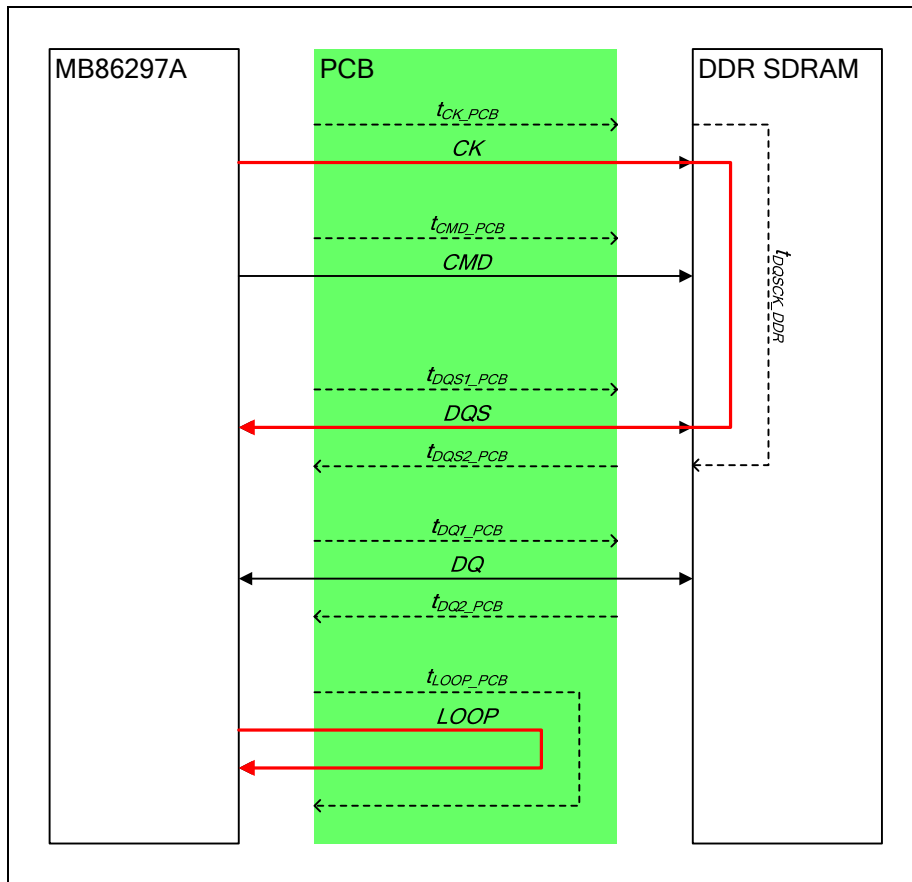


Figure 3 DQS Round Trip Time and LOOP Round Trip Time

$$(9) \quad t_{CK_PCB} + t_{DQSK_DDR_MIN} + t_{DQS2_PCB} > t_{RTT_DQS_MIN}$$

$$(10) \quad t_{CK_PCB} + t_{DQSK_DDR_MAX} + t_{DQS2_PCB} < t_{RTT_DQS_MAX}$$

LOOP Round Trip Time:

$$(11) \quad t_{RTT_LBCK_MIN} < t_{LOOP_PCB} < t_{RTT_LBCK_MAX}$$

Please note that $t_{RTT_LBCK_MIN}$ has a negative value in the CHWRM. Since the PCB delay is always positive, the left part of (11) is always fulfilled.

Difference between LOOP Round Trip Time and DQS Round Trip Time:

$$(12) \quad t_{CK_PCB} + t_{DQSK_DDR_MIN} + t_{DQS2_PCB} - t_{LOOP_PCB} > t_{Skew_LP_CLK_MIN}$$

$$(13) \quad t_{CK_PCB} + t_{DQSK_DDR_MAX} + t_{DQS2_PCB} - t_{LOOP_PCB} < t_{Skew_LP_CLK_MAX}$$

Appendix A Tested DDR SDRAMs

Theoretically, the MB86297A 'Carmine' graphics controller should work with any JEDEC-compliant DDR SDRAM.

Table 2 lists DDR SDRAMs that have been successfully tested in hardware together with the MB86297A 'Carmine'

Manufacturer	Type	Size	Comment
Samsung	K4H561638F-UC	16Mx16	Used on MB86297A 'Carmine' PCI evaluation board

Table 2 Tested DDR SDRAMs