

Application Note



MB86287 “Carminé” PCI Interface

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History

Date	Author	Version	Comment
11.10.2005	AG	1.0	First version

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1 PCI timing for 33MHz and 66 MHz

Symbol	Parameter	66 MHz		33 MHz ⁷		Units	Notes
		Min	Max	Min	Max		
T _{val}	CLK to Signal Valid Delay - bused signals	2	6	2	11	ns	1, 2, 3, 8
T _{val(ptp)}	CLK to Signal Valid Delay - point to point signals	2	6	2	12	ns	1, 2, 3, 8
T _{on}	Float to Active Delay	2		2		ns	1, 8, 9
T _{off}	Active to Float Delay		14		28	ns	1, 9
T _{su}	Input Setup Time to CLK - bused signals	3		7		ns	3, 4, 10
T _{su(ptp)}	Input Setup Time to CLK - point to point signals	5		10,12		ns	3, 4
T _h	Input Hold Time from CLK	0		0		ns	4
T _{rst}	Reset Active Time after power stable	1		1		ms	5
T _{rst-clk}	Reset Active Time after CLK stable	100		100		µs	5
T _{rst-off}	Reset Active to output float delay		40		40	ns	5, 6
t _{rsu}	REQ64# to RST# setup time	10T _{cyc}		10T _{cyc}		ns	
t _{rth}	RST# to REQ64# hold time	0	50	0	50	ns	
T _{rhfa}	RST# high to first Configuration access	2 ^m		2 ^m		clocks	
T _{rhff}	RST# high to first FRAME# assertion	5		5		clocks	

Figure 1 33MHz/66MHz timing

Note 8:

When M66EN is asserted, the minimum specification for T_{val}, T_{val} and T_{on} may be reduced to 1ns if a mechanism is provided to guarantee a minimum value of 2ns when M66EN is deasserted.

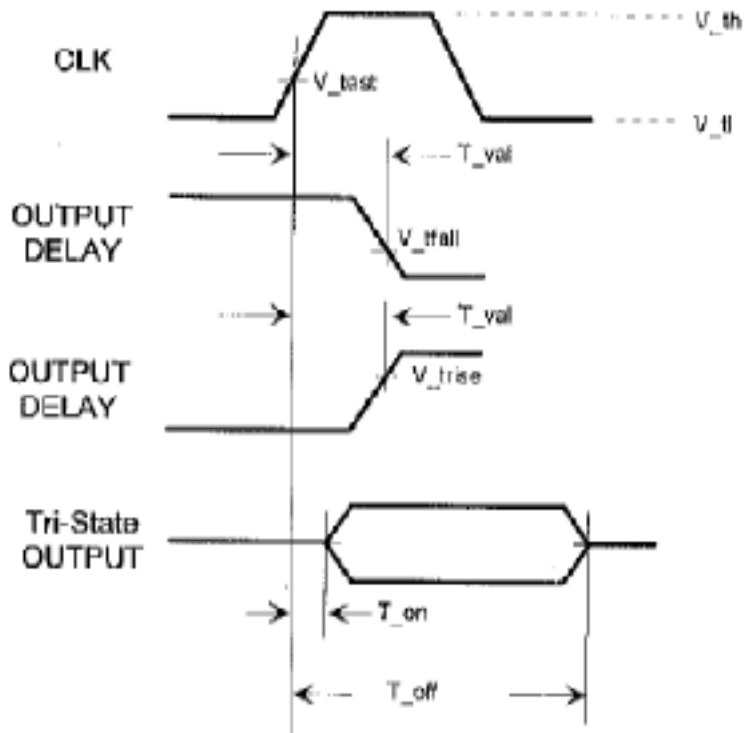


Figure 2 timing diagram

2 Carmine specification

The timing specification of PCI bus is conform to PCI-66 specifications. Especially about output delay T_{val} (Figure 1), the target specification is Min.1ns / Max.6ns. But the PCI-specification requires Min.2ns for 33MHz.

2.1 Operating the Carmine with 66 MHz

The Carmine timing is conform to the 66MHz-PCI-specification. M66EN should be asserted.

2.2 Operating the Carmine with 33 MHz

The Carmine does not fulfil the PCI-specification for 33MHz. In that case the hardware design has to adjust the timing values according to the Carmine specification.

The 33MHz-PCI-specification requires a minimum delay value (T_{val}) of 2 ns. It is recommended to delay data signals with external bus logic by 1 ns.