

Application Note



MB86287 “Carminé” Jitter at the DOTCLK

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History

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14/06/2006	AG	1.0	First version

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0 Calculating the period jitter value for the DOTCLK signal

Referring to the table 9.20 of the Carmine hardware manual rev. 0.72 the jitter value of the PLL output is defined with 47 ps.

The jitter for the DOTCLK signal depends on the scaling value what is set to the DCM0/DCM1 register. It is calculated basing on the following formula, what is valid for 90 nm technology:

j_{DOTCLK} : jitter value at the DOTCLK
 j_{PLL} : jitter at PLL output
 N : scaling value

$$j_{\text{DOTCLK}} = j_{\text{PLL}} \times \text{SQRT}(N) = 47 \text{ ps} \times \text{SQRT}(N)$$

e.g.:

The maximum jitter occurs with N_{max} .

$$N_{\text{max}} = 64$$

DCLKO frequency is $526,5\text{MHz}/64 = 8,2\text{MHz}$

$$47\text{ps} \times \text{SQRT}(64) = 47\text{ps} \times 8 = 376\text{ps}$$

The period jitter is the jitter value, what can occur between any 2 periods of the DOTCLK.