

# Application Note



## Video Capture

### MB86276 'Lime'

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#### History

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23.10.2007	AvT	V1.00	First version

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# 1 Capturing external video with MB86276 'Lime'

This application note covers the following topics:

- video capture in single buffer mode
- use of a video capture image as a (video) texture

The document explains which registers are used to sync the video capture with the external VSYNC signal and describes the basic handling in a system.

## 1.1 Use of Capture VSYNC (VS) Interrupt

The VS interrupt flags the VSYNC timing of a video signal being captured. The status register in the corresponding capture controller is the CINT register.

This interrupt is used with the following intentions:

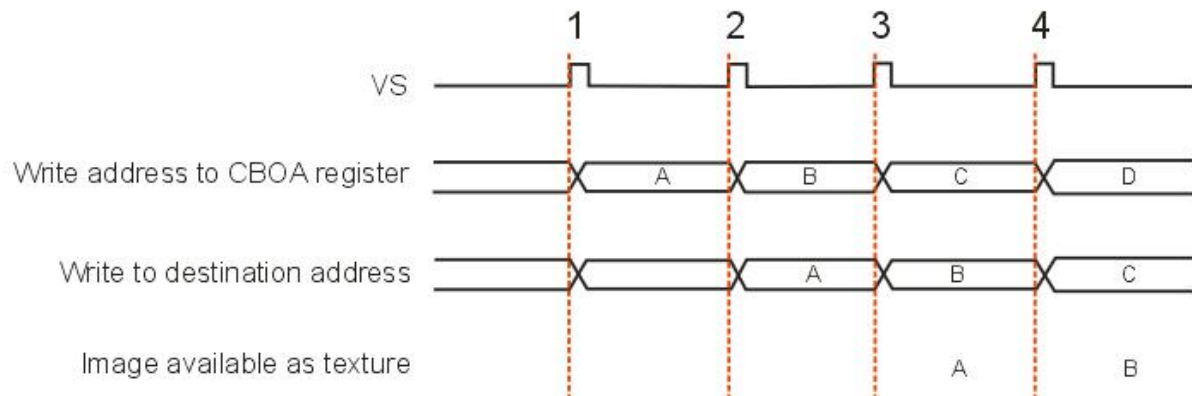
- (1) Detection of end of valid image (field) input
- (2) Frame management by the host CPU

'Single buffer mode' is the term used when the buffer is *not* a ringbuffer (i.e. *not* an area of memory that is wrapped around and overwritten). A software-managed setup uses single buffer mode. The registers used to specify the address parameters of the buffer are:

- ❑ CBOA (Capture Buffer Origin Address, holds the starting address of the destination buffer)
- ❑ CBLA (Capture Buffer Limit Address, states the end of a buffer)

These registers can be rewritten after the VSYNC (VS) interrupt has occurred.

When the VS interrupt occurs, the frame is immediately written to the address held in CBOA. The address is then changed (before the next VS interrupt) but the new address will only become effective at the next frame interrupt (VS). In other words, the captured image at the previous address can be used as a still image for texturing.



Note: In single buffer operating mode, set the CBOA and CBLA registers to the same value.

## 1.2 Video Capture Registers

### *CINT*(Capture Interrupt)

Register address	CaptureBaseAddress + 178 <sub>H</sub>																															
Bit No.	31:30:29:28:27:26:	21:20:19:18:17:16:15:14:13:12:11:10:9:8:7:6:5:4:3:2:	1	0																												
Bit field name	Reserved																														VS	
R/W	R																														RW0	
Initial value	0																														0	

This register is the video synchronization signal interrupt status register. The register is cleared by writing "0" to it.

Bit 1 VS (VSYNC)  
 1: VSYNC  
 0: No VSYNC

### *CINTMASK* (Capture Interrupt Mask)

Register address	CaptureBaseAddress + 17C <sub>H</sub>																															
Bit No.	31:30:29:28:27:26:	21:20:19:18:17:16:15:14:13:12:11:10:9:8:7:6:5:4:3:2:	1	0																												
Bit field name	Reserved																														VS	
R/W	R																														RW	
Initial value	0																														0	

This register masks the video synchronization signal interrupt

Bit 1 VS (VSYNC)  
 1: Do not mask VS interrupt.  
 0: Masks VS interrupt.

### 1.3 Notes

The host interface interrupt is operated by the IST/IMASK registers in the same way as other interrupts. Bit16 of each register is assigned to this purpose. The video capture module has its own interrupt registers: the Cint/CintMask registers.

Host IF registers:

- 1) Interrupt flag  
Bit16 of the IST register
- 2) Interrupt mask  
Bit16 of the IMASK register

Video Capture registers:

(Note: these are currently not described in the current MB86276 'Lime' Hardware Manual, Rev. 1.00)

- 1) Capture field interrupt state  
CINT (offset = 0x178) bit1
- 2) Capture field interrupt mask  
CINTMASK (offset = 0x17c) bit1

The reset (default) register setup is as follows:

- Bit1 of the CINT register is cleared
- Bit16 of the IST register is cleared
- Bit16 of the IMASK register is set to 1
- Bit1 of the CINTMASK register is set to 1

On an interrupt the following actions are necessary (in this order):

- Clear Bit1 of the CINT register
- Clear Bit16 of the IST register
- Execute operations as necessary

When you clear an event that has been acknowledged, you must clear the flag of the Cint register *before* clearing Bit16 of the IST register.

It is also possible to poll the interrupt flags. In this case, you should use a mask value of 0 for the respective bits (i.e. don't mask them out): Bit1 of the IMASK register and Bit1 of the CINTMASK register.