

	Pin Name	Direction *1	State after reset	Default Treatment	Treatment of unused *2	Comment
Host Interface	MODE0-2	I	Input	Connect to VDDH or GND according to the CPU mode.	<=	See "4 HOST INTERFACE"
	RDY_MODE	I	Input	Connect to VDDH or GND according to the Ready signal mode.	<=	See "4 HOST INTERFACE"
	BS_MODE	I	Input	Connect to VDDH or GND according to the BS signal mode.	<=	See "4 HOST INTERFACE"
	D0-15	IO	Input	Connect to CPU data bus.	<=	
	D16-31	IO	(indefinite)	Connect to CPU data bus.	select according to the	See "2.3 Pin multiplex table"
	A2-A25	I	(indefinite)	Connect to CPU address bus.	select according to the	See "2.3 Pin multiplex table"
	BCLK1	I	Input	Connect to CPU bus clock.	<=	Input the clock when power-on. See "14.3.2 Note at power-on"
	XBS	I	Input	Connect to CPU bus cycle start indicating signal.	When MODE2=L and BS_MODE=H, PullUp	This signal is 1 shot BCLK1 pulse that indicates the bus cycle start.
	XCS	I	Input	Connect to chip select signal	<=	
	XRD	I	Input	Connect to CPU read strobe signal	<=	
	XWEO-XWE3	I	Input	Connect to CPU write byte enable signals.	<=	Connect byte enable signal in V832 mode.
	XRDY	O(T)	Hi-Z	Connect to CPU Ready (Wait) signal and Pull Up/Down according to	<=	See "4 HOST INTERFACE"
	DREQ	O	High	Connect to CPU DREQ signal	OPEN	SH3/4,V832=Low Active, See "4.2 DMA Transfer"
DRACK/DMAAK	I	Input	Connect to CPU DRACK signal	PullDown	Connect to DMAAK signal in V832 Mode, SH3/4,V832=High Active, See "4.2 DMA Transfer"	
DTACK/XTC	I	Input	Connect to CPU DTACK signal	V832=PullUp, the others=PullDown	Connect to XTC signal in V832 mode, SH3/4=High Active, V832=Low Active, See "4.2 DMA Transfer"	
XINT	O	(indefinite)	Connect to CPU interrupt signal	OPEN	SH3/4=Low Active, V832=High Active	
Video Output Interface	DCLK0	O	Clock	Connect to dot clock	<=	Selectable clock source, DCLKI or output of internal PLL. See DCM0/1 Register in "12.3 Display control registers"
	R07-0	O	(indefinite)	Connect to R video signals.	OPEN	
	G07-0	O	(indefinite)	Connect to G video signals.	OPEN	
	B07-0	O	(indefinite)	Connect to B video signals.	OPEN	
	DCLKI	I	Input	Connect to clock for dot clock	PullDown	
	HSYNC	IO	Input	Connect to HSYNC signal and Pull Up	<=	
	VSYNC	IO	Input	Connect to VSYNC signal and Pull Up	<=	
	CSYNC	O	(indefinite)	Connect to CSYNC signal	OPEN	
	DISPE	O	(indefinite)	Connect to Display enable signal	OPEN	
GV	O	(indefinite)	Connect to select signal or analog video	OPEN	GDC's display = High Level	
Video Capture Interface	RGBCLK	I	Input	Connect to clock for capture	<=	
	RIO-5	I	Input	Connect to R capture data.	PullUp	
	GIO-5	I	Input	Connect to G capture data.	PullUp	
	BIO-5	I	Input	Connect to B capture data.	PullUp	
	VSYNCI	I	Input	Connect to capture's VSYNC signal	PullUp	
	HSYNCI	I	Input	Connect to capture's HSYNC signal	PullUp	
	VINFID	I	Input	Connect to capture's field identification signal	PullUp	(unpublished specification, it doesn't work)
Graphics Memory Interface	MD0-MD31	IO	High	Connect to graphics memory data bus.	<=	
	MA0-MA14	O	(indefinite)	Connect to graphics memory address and bank signals.	Unused upper pins => OPEN	
	MRAS	O	(indefinite)	Connect to graphics memory row address strobe signal.	<=	
	MCAS	O	(indefinite)	Connect to graphics memory column address strobe signal.	<=	
	MWE	O	(indefinite)	Connect to graphics memory write enable signal.	<=	
	MDSM0-MDSM10	O	(indefinite)	Connect to graphics memory data mask	<=	
	MCLK0	O	(indefinite)	Connect to graphics memory clock and MCLKI	<=	
MCLKI	I	Input	Connect to MCLK0*3	<=		
I2C Interface	SDA	IO	Input	Connect to SDA signal and Pull Up	PullUp	See "2.8 I2C Interface"
	SCL	IO	Input	Connect to SCL signal and Pull Up	PullUp	See "2.8 I2C Interface"
GPIO Interface	GPIO0-4	IO	Input		PullUp	See "2.9 GPIO Interface"
Clock/System	CLKSELO-1	I	Input	Connect to GND or VDDH according to the input frequency to CLK	<=	See "2.11 Clock Input"
	CLK	I	Input	Input a clock according to the setting of CLKSEL1-0	<=	See "2.11 Clock Input", "14.3.2 Note at power-on". Input the clock when power-on
	XRST	I	Input	Input hardware reset signal	<=	See "3 PROCEDURE OF THE HARDWARE INITIALIZATION", "14.3.2 Note at power-on". XRST has to be Low level when power-on.
	S	I	Input	Input PLL reset	<=	See "2.11 Clock Input", "14.3.2 Note at power-on". S has to be Low level when power-on.
	CKM	I	Input	Select High/Low according to the mode.	<=	See "2.11 Clock Input"

Note) This device is warranted under the above listed condition. No warranty made with other combination or treatments.

Semiconductor devices fail with a known probability. Customer must use safety design (such as redundant design, fire proof design, over current prevention design, and malfunction prevention design) so that failures will not cause accidents, injury or death.

*1: I=Input pin, O=Output pin, O(T)= Output Tri-state pin, IO=Bi-directional pin

*2: "<=" mark means treat a pin same as default

*3: Recommend to be same length MCLKI to A, MCLK0 to A, SDRAM CLK to A and take care the AC spec of graphics memory interface.

