

DMA Function in 16-bit Mode

MB86276 'Lime'

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History

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1 DMA Function in 16-Bit Mode

It is possible to use DMA controller of the CPU to transfer data to Lime in the 16bit SRAM, 16bit A/D multiplex and 32bit A/D multiplex modes. However, unlike the legacy 32-bit modes (SH3, SH4 etc.), there is no 'special' access mode for DMA in these configurations. The timing diagram for DMA access is same as the normal CPU access. The signals DREQ, DACK, and DTACK are not required.

1.1 DMA Access to Lime in 16bit SRAM I/F and 16bit A/D Multiplex Modes

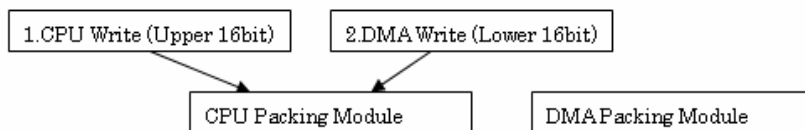
In 16bit SRAM and 16bit A/D mux mode, the access to Lime has to be done using continuous addresses for the sake of correctly packing the 16bit data to 32bit data size internally. There are separate packing modules for CPU and DMA accesses. For the sake of example, we can consider a CPU access for a Lime register and a DMA access may be for transferring a bitmap to VRAM. Since the two types of accesses can occur one after the other, Lime needs to know whether the address and data existing on the host interface is for the CPU access or the DMA access. After correctly specifying Lime's DMA destination area in the following registers, Lime will be able to identify that.

- DMA_ST_ADR(HostBase+0x500): DMA access start address
- DMA_ED_ADR(HostBase+0x504): DMA access end address

An address that falls within the range specified by these registers will be considered a DMA access; otherwise it will be a CPU access. Consequently, the data will be sent to the correct packing module and then on to the correct location within Lime. In our example, the data for regular CPU access will end up in a register and that for the DMA access in the VRAM.

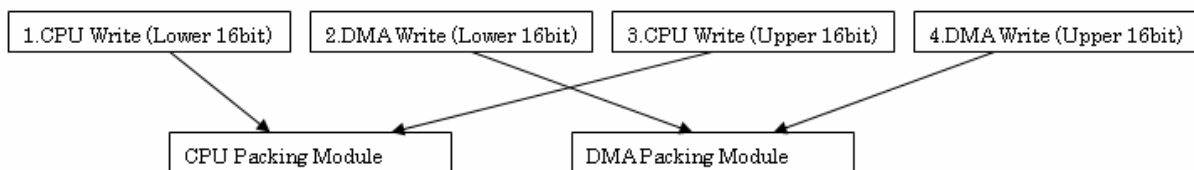
1.2 Examples

Example 1: CPU write and DMA write *without setting* DMA_ST_ADR, DMA_ED_ADR.



In this case, both CPU and DMA write are NOT processed correctly. The CPU and DMA data are packed together into one chunk of 32-bit data for the CPU access address.

Example 2: CPU write and DMA write *with setting* DMA_ST_ADR, DMA_ED_ADR.



Both CPU and DMA write are packed correctly by the respective packing modules