

## Clock Generation - Coral Series

### MB86276 'Lime'

© Fujitsu Microelectronics Europe GmbH

#### History

Date	Author	Version	Comment
01.05.2007	AvT	V1.00	First version
09.05.2007	AvT	V1.01	Correction to DCLKI (max. 80 MHz), new diagram

## Warranty and Disclaimer

To the maximum extent permitted by applicable law, Fujitsu Microelectronics Europe GmbH restricts its warranties and its liability for **all products delivered free of charge** (e.g. software include or header files, application examples, target boards, evaluation boards, engineering samples of IC's etc.), its performance and any consequential damages, on the use of the Product in accordance with (i) the terms of the License Agreement and the Sale and Purchase Agreement under which agreements the Product has been delivered, (ii) the technical descriptions and (iii) all accompanying written materials. In addition, to the maximum extent permitted by applicable law, Fujitsu Microelectronics Europe GmbH disclaims all warranties and liabilities for the performance of the Product and any consequential damages in cases of unauthorised decompiling and/or reverse engineering and/or disassembling.

**Note that all these products are intended and must only be used in an evaluation laboratory environment.**

1. Fujitsu Microelectronics Europe GmbH warrants that the Product will perform substantially in accordance with the accompanying written materials for a period of 90 days from the date of receipt by the customer. Concerning the hardware components of the Product, Fujitsu Microelectronics Europe GmbH warrants that the Product will be free from defects in material and workmanship under use and service as specified in the accompanying written materials for a duration of 1 year from the date of receipt by the customer.
2. Should a Product turn out to be defect, Fujitsu Microelectronics Europe GmbH's entire liability and the customer's exclusive remedy shall be, at Fujitsu Microelectronics Europe GmbH's sole discretion, either return of the purchase price and the license fee, or replacement of the Product or parts thereof, if the Product is returned to Fujitsu Microelectronics Europe GmbH in original packing and without further defects resulting from the customer's use or the transport. However, this warranty is excluded if the defect has resulted from an accident not attributable to Fujitsu Microelectronics Europe GmbH, or abuse or misapplication attributable to the customer or any other third party not relating to Fujitsu Microelectronics Europe GmbH.
3. To the maximum extent permitted by applicable law Fujitsu Microelectronics Europe GmbH disclaims all other warranties, whether expressed or implied, in particular, but not limited to, warranties of merchantability and fitness for a particular purpose for which the Product is not designated.
4. To the maximum extent permitted by applicable law, Fujitsu Microelectronics Europe GmbH's and its suppliers' liability is restricted to intention and gross negligence.

### **NO LIABILITY FOR CONSEQUENTIAL DAMAGES**

**To the maximum extent permitted by applicable law, in no event shall Fujitsu Microelectronics Europe GmbH and its suppliers be liable for any damages whatsoever (including but without limitation, consequential and/or indirect damages for personal injury, assets of substantial value, loss of profits, interruption of business operation, loss of information, or any other monetary or pecuniary loss) arising from the use of the Product.**

Should one of the above stipulations be or become invalid and/or unenforceable, the remaining stipulations shall stay in full effect

# Contents

- Warranty and Disclaimer ..... 2
- 1 Clock Generation Module..... 4
  - 1.1 Clock for Other Modules (Rendering Engine) ..... 4
  - 1.2 Clock for Video Output ..... 4

# 1 Clock Generation Module

The clock generation module of the MB86276 'Lime' graphics controller provides the separate clock signals required by:

- various modules (e.g. rendering engine) and the memory interface (memory clock)
- the video output unit (dot clock)

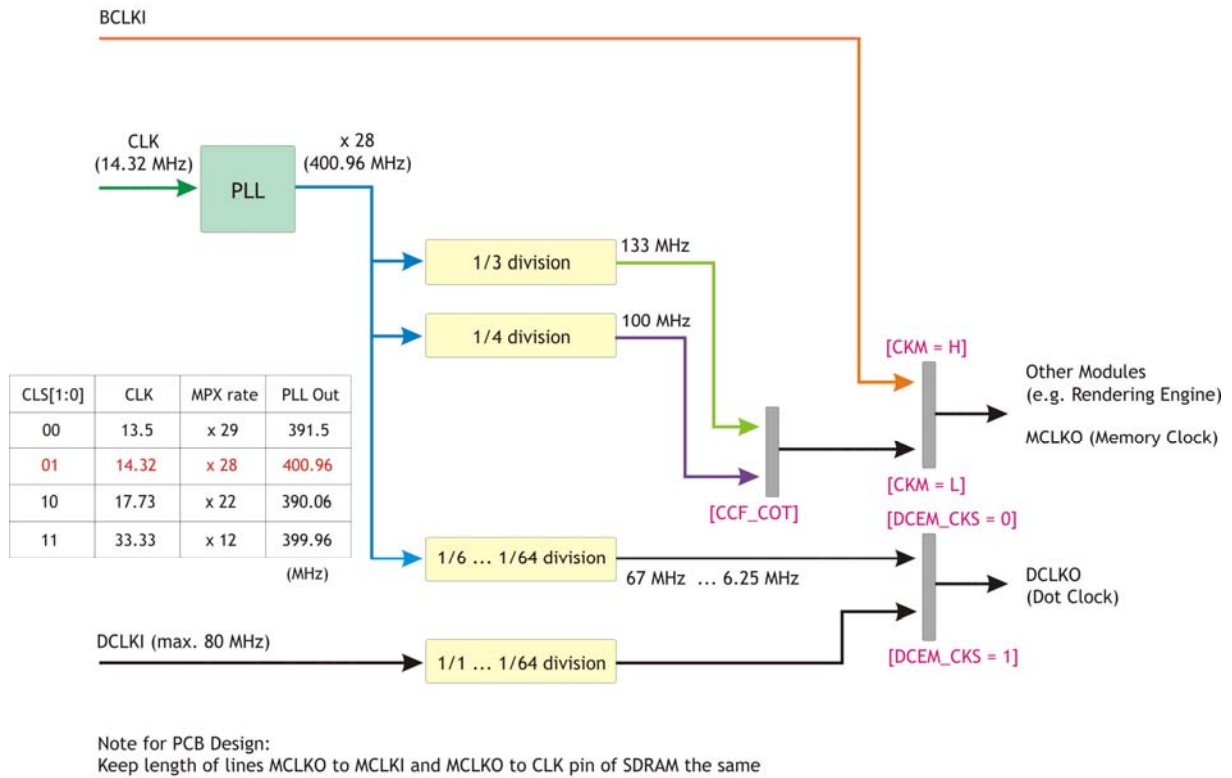


Figure 1 Clock Generation Module

## 1.1 Clock for Other Modules (Rendering Engine)

The CKM (Clock Mode) pin determines which of two basic input clock signals is used.

CKM Pin State	Clock used
CKM = H	BCKLI (PCI bus clock)
CKM = L	Internal PLL

The internal PLL generates an internal clock signal with a frequency of 400.96 MHz when it is clocked by an external 14.32MHz-oscillator.

If the internal PLL is used to generate the clock signal for the other modules (e.g. rendering engine) and for the memory clock, the final frequency (133 or 100 MHz) is set by the COT bitfield of the CCF (Change of Clock Frequency) register (host base address +0x38). Please refer to the Hardware Manual for more details.

## 1.2 Clock for Video Output

The frequency of the dot clock signal for video output is set via the DCM0 (Display Control Module) register. This register can be accessed via 2 addresses , either DispBaseAddress + 0x00 or via DispBaseAddress + 0x100.

The interpretation of the SC (scaling) bitfield of this register which is used to divide the display reference clock by the preset ratio (in order to generate the dot clock signal) depends on whether this register was accessed by + 0x00 or + 0x100.

The output frequency is calculated by either:

- $f_{\text{dot\_clk}} = f_{\text{ref}} / (2 * (\text{SC} + 1))$  if this register is accessed via offset 0x00 or
- $f_{\text{dot\_clk}} = f_{\text{ref}} / (\text{SC} + 1)$  if this register is accessed via offset 0x100

Furthermore, the CKS bit of this register selects the input reference clock source ( $f_{\text{ref}}$ ). This source can be either the internal PLL clock or the clock signal on pin DCLKI.

Access to DCM0 register @DispBase + Offset = 0x00			Access to DCM0 register @DispBase + Offset = 0x100		
scaler SC	Calculated frequency [MHz] $f_{\text{dot\_clk}} = f_{\text{ref}} / (2 * (\text{SC} + 1))$ $f_{\text{ref}} = 400\text{MHz}$	Measured frequency [MHz]	scaler SC	Calculated frequency [MHz] $f_{\text{dot\_clk}} = f_{\text{ref}} / (\text{SC} + 1)$ $f_{\text{ref}} = 400\text{MHz}$	Measured frequency [MHz]
0	400.00	80 <sup>*)</sup>	0	400.00	80 <sup>*)</sup>
1	100.00	50 <sup>*)</sup>	1	200.00	66.8 <sup>*)</sup>
2	66.67	67.67	2	133.33	56.8 <sup>*)</sup>
3	50.00	50.00	3	100.00	50 <sup>*)</sup>
4	40.00	40.16	4	80.00	80.65 <sup>*)</sup>
5	33.33	33.33	5	66.67	66.67
6	28.57	28.57	6	57.14	57.50
7	25.00	25.00	7	50.00	50.00
8	22.22	22.27	8	44.44	44.60
9	20.00	20.04	9	40.00	40.00
10	18.18	18.21	10	36.36	36.40
11	16.67	16.70	11	33.33	33.40
12	15.38	15.46	12	30.79	30.70
13	14.29	14.31	13	28.57	28.65
14	13.33	13.35	14	26.67	26.80
15	12.50	12.53	15	25.00	25.00
16	11.76	11.79	16	23.52	23.58
17	11.11	11.14	17	22.22	22.22
18	10.53	10.53	18	21.05	21.10
19	10.00	10.02	19	20.00	20.00
20	9.52	9.50	20	19.04	19.09
21	9.09	9.01	21	18.18	18.20
22	8.70	8.71	22	17.39	17.40
23	8.33	8.35	23	16.66	16.70
24	8.00	8.00	24	16.00	16.03
25	7.69	7.71	25	15.38	15.40
26	7.41	7.42	26	14.81	14.82

78	7.14	7.16		27	14.28	14.32
28	6.90	6.91		28	13.79	13.82
29	6.67	6.67		29	13.33	13.35
30	6.45	6.46		30	12.90	12.95
31	6.25	6.26		31	12.50	12.52
				32	12.12	
				33	11.76	
				34	11.42	
				35	11.11	
				36	10.81	
				37	10.53	
				38	10.26	
				39	10	
				40	9.76	
				41	9.52	
				42	9.3	
				43	9.09	
				44	8.89	
				45	8.69	
				46	8.51	
				47	8.33	
				48	8.16	
				49	8	
				50	7.84	
				51	7.69	
				52	7.54	
				53	7.41	
				54	7.27	
				55	7.14	
				56	7.01	
				57	6.89	
				58	6.77	
				59	6.67	
				60	6.56	
				61	6.45	
				62	6.35	
				63	6.25	

Only 5 SC-bits @ offset 0

**Table 1 Video Output Frequency**