

## MB86276 'Lime' Interfacing to CPU's (Bus Modes)

© Fujitsu Microelectronics Europe GmbH

### History

Date	Author	Version	Comment
17.03.2009	AvT	1.00	First version

## Warranty and Disclaimer

To the maximum extent permitted by applicable law, Fujitsu Microelectronics Europe GmbH restricts its warranties and its liability for **all products delivered free of charge** (eg. software include or header files, application examples, **Application Notes**, target boards, evaluation boards, engineering samples of IC's etc.), its performance and any consequential damages, on the use of the Product in accordance with (i) the terms of the License Agreement and the Sale and Purchase Agreement under which agreements the Product has been delivered, (ii) the technical descriptions and (iii) all accompanying written materials. In addition, to the maximum extent permitted by applicable law, Fujitsu Microelectronics Europe GmbH disclaims all warranties and liabilities for the performance of the Product and any consequential damages in cases of unauthorised decompiling and/or reverse engineering and/or disassembling. **Note, all these products are intended and must only be used in an evaluation laboratory environment.**

1. Fujitsu Microelectronics Europe GmbH warrants that the Product will perform substantially in accordance with the accompanying written materials for a period of 90 days from the date of receipt by the customer. Concerning the hardware components of the Product, Fujitsu Microelectronics Europe GmbH warrants that the Product will be free from defects in material and workmanship under use and service as specified in the accompanying written materials for a duration of 1 year from the date of receipt by the customer.
2. Should a Product turn out to be defect, Fujitsu Microelectronics Europe GmbH's entire liability and the customer's exclusive remedy shall be, at Fujitsu Microelectronics Europe GmbH's sole discretion, either return of the purchase price and the license fee, or replacement of the Product or parts thereof, if the Product is returned to Fujitsu Microelectronics Europe GmbH in original packing and without further defects resulting from the customer's use or the transport. However, this warranty is excluded if the defect has resulted from an accident not attributable to Fujitsu Microelectronics Europe GmbH, or abuse or misapplication attributable to the customer or any other third party not relating to Fujitsu Microelectronics Europe GmbH.
3. To the maximum extent permitted by applicable law Fujitsu Microelectronics Europe GmbH disclaims all other warranties, whether expressed or implied, in particular, but not limited to, warranties of merchantability and fitness for a particular purpose for which the Product is not designated.
4. To the maximum extent permitted by applicable law, Fujitsu Microelectronics Europe GmbH's and its suppliers' liability is restricted to intention and gross negligence.

### **NO LIABILITY FOR CONSEQUENTIAL DAMAGES**

**To the maximum extent permitted by applicable law, in no event shall Fujitsu Microelectronics Europe GmbH and its suppliers be liable for any damages whatsoever (including but without limitation, consequential and/or indirect damages for personal injury, assets of substantial value, loss of profits, interruption of business operation, loss of information, or any other monetary or pecuniary loss) arising from the use of the Product.**

Should one of the above stipulations be or become invalid and/or unenforceable, the remaining stipulations shall stay in full effect.

# 1 Foreword

This document describes how to connect MB86276 'Lime' to an external CPU. This application note **exclusively** describes implementations that currently exist as working applications (i.e. are fully functional). Other CPU interfacing solutions exist within the functional scope of the GDC but are not described here. Such applications may be operational but require additional external glue logic etc.

## 2 Interfacing Lime to an external CPU

### 2.1 General Notes

Lime has been successfully tested and approved as fully functional in both 16-bit and 32-bit non-multiplexed applications.

### 2.2 Compatible CPU's

The following CPU's have been successfully used in solutions together with MB86276 'Lime' in 32-bit or 16-bit non-multiplexed modes:

- MB91F46x - Fujitsu Evaluation Boards:
  - SK-86276-91F467D  
(MCU in 32 bit mode, Lime in 32 bit mode, bus usage via 2x16 bit accesses)  
(see <http://www.fujitsu.com/emea/services/microelectronics/gdc/evalbds/lime-467-evalboard.html>)
  - CREMSON-STARTERKIT-CPU369 + CREMSON-STARTERKIT-LIME  
(MCU in 32 bit mode + Lime in 32 bit mode)  
(see <http://www.fujitsu.com/emea/services/microelectronics/gdc/gdcdevices/mb86276-lime.html#development-tools>)
  - SK-91F467D-208PFV + CREMSON-STARTERKIT-LIME  
(MCU in 32 bit mode + Lime in 32 bit mode)  
(see <http://www.fujitsu.com/emea/services/microelectronics/gdc/gdcdevices/mb86276-lime.html#development-tools>)

Other proprietary applications using non-Fujitsu CPU's (examples are listed below) exist on the market (e.g. the MPX5200G from Microsys, see <http://www.microsys.de/MPX5200G.htm>), but these require and implement additional glue logic to interface with MB86276 'Lime':

- Arm7
- MPC5200
- M16C

## 2.3 Physical Connections to external CPU's

Lime registers are always 32 bits wide and access therefore using 32 bits. 16 bit mode is supported by Lime using 2x 16 bit access (for 32 bits).

The address signal is 32 bits (per one double-word) × 24, and has a 64-Mbyte address field. (16-MByte address space is provided for V832 and SPARClite.)

The external bus operating frequency is up to 66 MHz.

In the SH4, V832, and SPARClite modes, when the XRDY signal is low, it is in the ready state. However, in the SH3 mode, when the XRDY signal is low, it is in the wait state. This signal is a tri-state output that is synchronized with the rising edge of BCLKI.

DMA data transfer is supported using an external DMA controller.

An interrupt signal is generated to the host CPU.

The XRST input must be kept low for at least 300 μs after setting the S (PLL reset) signal to high.

How to connect between Lime and CPUs is shown as the following table.

Pin name	In/Out	SH4(SH7750)	SH3(SH7709)	V832
BCLKI	I	CKIO	CKIO	CLKOUT
A3-A0	I	A5-A2	A5-A2	A5-A2
A11-A4	I	A13-A6	A13-A6	A13-A6
A19-A12	I	A21-A14	A21-A14	A21-A14
A21-A20	I	A23-A22	A23-A22	A23-A22
A22	I	A24	A24	-
A23	I	A25	A25	-
XCS	I	CSn	CSn	CSn
D15-0	IO	D15-D0	D15-D0	D15-D0
D31-16	IO	D31-D16	D31-D16	D31-D16
XRD	I	RD	RD	IORD/MRD
XWE0	I	WE <sub>n</sub>	WE <sub>n</sub>	IOWR/xxBEN/MWR
XWE1	I			
XWE2	I			
XWE3	I			
XBS	I	BS	BS	BCYST
XRDY	O	RDY	WAIT	READY
DREQ	O	DREQ	DREQ	DMARQ
DRACK	I	DRAK	DRAK	DMAAK
DTACK	I	DACK	DACK	XTC
XINT	O			
MODE0-2	I			
RDY_MODE	I			
BS_MODE	I			

Pin name	In/Out	MB91F46x (16-bit) non-MUX	MB91F46x (32-bit) non-MUX
BCLKI	I	SYSCLK	SYSCLK
A3-A0	I	A04-A01	A04-A01
A11-A4	I	A12-A05	A12-A05
A19-A12	I	A20-A13	A20-A13
A21-A20	I	A22-A21	A22-A21
A22	I	A23	A23
A23	I	-	-
XCS	I	CSnX	CSnX
D15-0	IO	D31-D16	D31-D16
D31-16	IO	-	-
XRD	I	IORDX	IORDX
XWE0	I	IOWRX	IOWRX
XWE1	I	-	-
XWE2	I	-	-
XWE3	I	-	-
XBS	I	ASX	ASX
XRDY	O	RDY	RDY
DREQ	O	-	-
DRACK	I	-	-
DTACK	I	-	-
XINT	O		
MODE0-2	I		
RDY_MODE	I		
BS_MODE	I		

Pin name	In/Out	MB90F38x 16-bit non-MUX
BCLKI	I	CLK
A0	I	Open
A8-A1	I	P11_7-P11_0
A15-A9	I	P12_6-P12_0
A20-A16	I	P03_3-P03_0
A23-A21	I	P08_6-P08_4
XCS	I	CS3
D7-D0	IO	P00_7-P00_0
D15-D8	IO	P02_7-P02_0
XRD	I	RDX
XWE0	I	WRLX
XWE1	I	WRHX
XWE2	I	-
XWE3	I	-
XBS	I	ALE / ASX
XRDY	O	RDY
DREQ	O	-
DRACK	I	-
DTACK	I	-
XINT	O	-
MODE0	I	GND
MODE1	I	GND
MODE2	I	VCC
RDY_MODE	I	GND
BS_MODE	I	GND
ENDIAN	I	GND
RDTSW	I	VCC