Fujitsu Microelectronics Europe
Application Note

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GRAPHIC CONTROLLER

CORAL FAMILY

Connection between Fujitsu Coral and Intel's X-Scale processor PXA250

APPLICATION NOTE

Revision History

Date	Issue
7.8.2002	V1.0, MM, WS First version created from an internal document by FMA (WS)

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Contents

0 Introduction

Graphic display controllers are an integral part of any graphic display system. They are used in both PC based systems and embedded display systems. Fujitsu's line of graphic display controllers has been designed specifically for the embedded applications e.g. a car navigation system. They exhibit the necessary features required in an automotive application like extended temperature range, EMI characteristics etc.

The application note will discuss Coral -- the latest in the series of 2D/3D graphic display controllers from Fujitsu, from the point of view of telematics applications. It will be an analysis of the connectivity between Fujitsu's Coral and Intel's X-Scale processor -- PXA250, which will act as a host processor. The following block diagram shows how the whole system can be arranged.

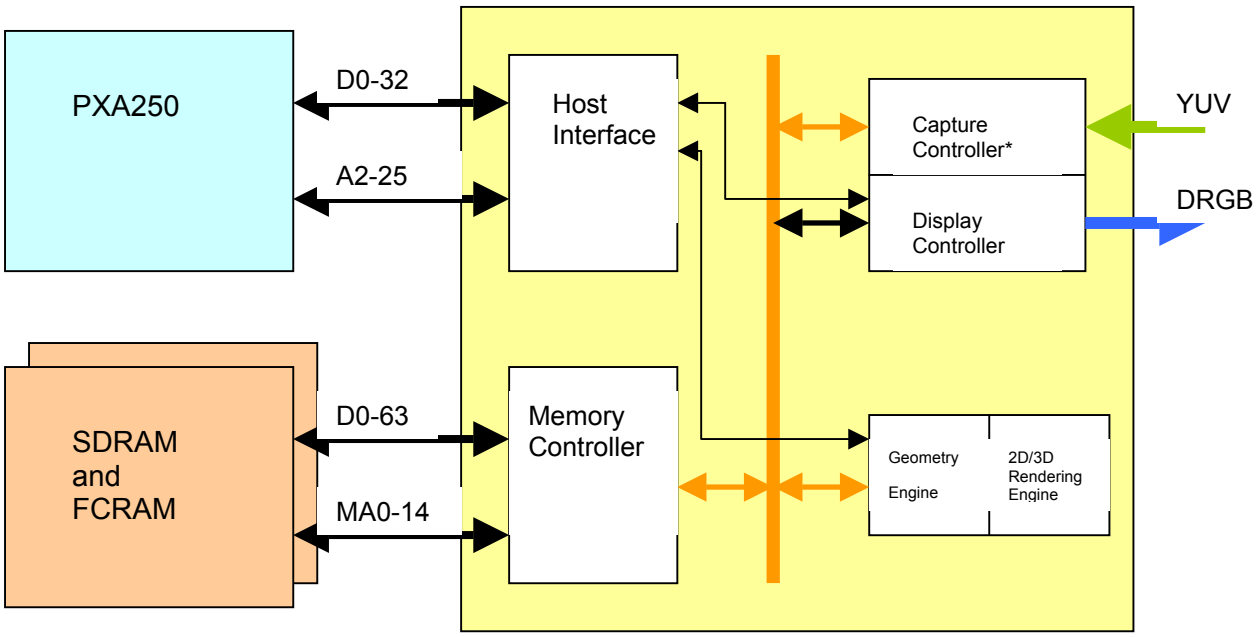

Fig 1. Coral Block Diagram

(Note: there are low end Coral versions that do not have a capture controller for video input)

*Will be available in selective versions

1 Coral (MB86293) Features

MB8629 "Coral", is the third generation of Fujitsu's graphic controllers following Cremson, Scarlet and Orchid. Coral will be the first graphic chip designed in 0.18um technology, which made it possible to implement many enhancements, such as 6 layers of overlay, 166MHz internal frequency for the geometry processor and 133MHz for other modules, true alpha-blending (using an alpha-plane), 24bpp color-depth for the display controller, multiple geometry-engines, new rendering features and much more. Coral will use external FCRAM or SDRAM memory of up to 64MB and a bus interface similar to Orchid. The video-scalar can also be used to enlarge images and is available in selective versions (please refer to Coral versions in the following table). The rendering features have been improved to fulfill the requirements of tomorrow's graphic-features: Texture-sizes can be up to 4096x4096 pixels, the speed of texture-mapping can be raised by a factor of 10, new features like BitBlt-Functions with alpha-blending, thick lines and patterned lines using 3D effects etc. Coral will be available in different packages and with different feature options.

Feature	Description
Voltage	3.3V (I/O) and 1.8V internal
Versions of Coral	High speed and low speed versions with/without vide capture function
Operating Temperature	-40 to +85 ^{o}C
Internal Frequency	166MHz for the geometry processor and 133MHz for other modules
Display Basic Clock	400MHz internal PLL clock
CPU Interface	Unmultiplexed Address and Data Lines, also supports DMA transfer, it has a 32-bit data bus with little endian mode
Graphics Memory Interface	Supports upto 8MB of FCRAM and 64MB of SDRAM
Video Input Format	ITU RBT-656 (YUV 422) **
Video Scaling	Supports both up-scaling and down-scaling for the video input *
Video Layers	6 layers that can be resized and arranged in any order, each of them can display captured video; two hardware cursors
Video Output	6/8-bit digital RGB output
Display Resolution	Upto XGA (1024x768)
2D/3D Rendering Functions	**2D**: 2D primitives, polygon drawing, BLT/rectangle fill, Pattern (text) drawing, clipping **3D**: 3D primitives, Hidden surface management, Anti-aliasing, line drawing, shadowing, alpha blending, shading (flat and gouraud), texture mapping
Geometry Processor	Primitives, MVP transformation, Clipping, Culling, 3D-2D transformation etc.

* Depends on the Coral version ** Will be available in selective versions

2 Connecting Coral with PXA250

The following figure shows how the different signals on Coral and PXA250 can be interfaced.

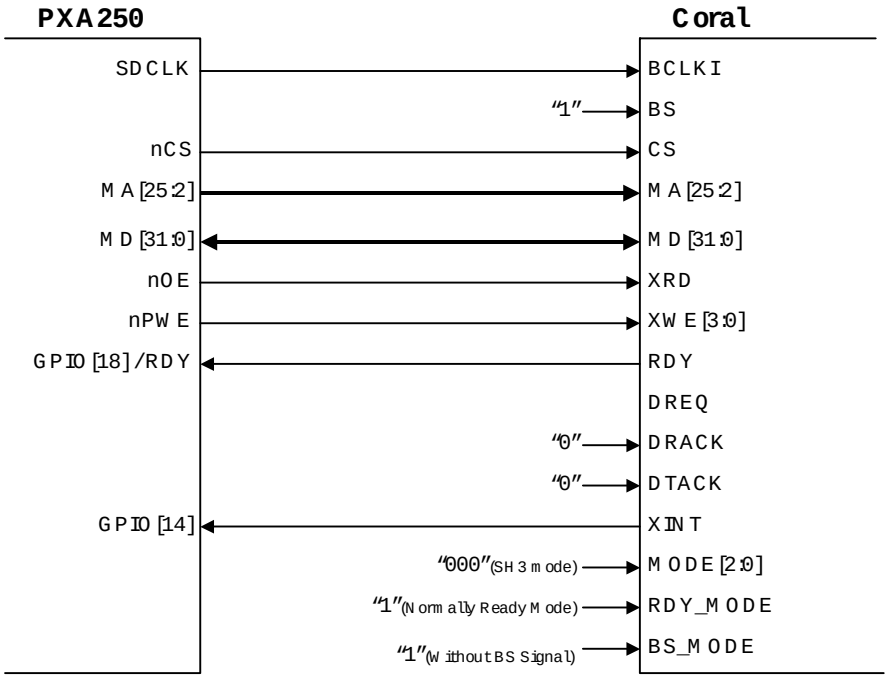

Fig 2. Coral and PXA250 connectivity diagram

Following is a summary of this interconnection,

- Both PXA250 and Coral have a data bus width of 32 bits.

- Both use an I/O voltage of 3.3V

- Coral's CPU interface can use both software wait and hardware wait (RDY signal). However, in PXA250, only the variable latency I/O interface mode allows an RDY signal for hardware wait. PXA250 can also use software wait by setting the RDNx bit of the MSCn register.

- Coral needs a "Bus start" signal of width equal to one BCLK pulse, to get information about bus access. However, the variable latency I/O interface does not provide this signal.

- The DMA Controller of PXA250 uses edge detection for the DREQ signal from other devices. However, the device connected to it is required to assert the DREQ signal for four MEMCLK cycles and, subsequently, must keep it de-asserted for another four MEMCLK cycles. In case of Coral, the DREQ signal is only one cycle wide.

- The interrupt signal from Coral (XINT) is low active in the SH3 mode, which will be used for this interconnection. PXA250's GPIO [14] can receive the interrupt signal and it can be set to Falling Edge Detect (GFER).

3 Conclusion

- Since, PXA250 does not offer any BS signal in the variable latency I/O interface mode, Coral must be used in a “non-BS signal mode”. However, the designer should take care of the “Soft wait length” and should set the value of RDNx to more than 4. Otherwise, signals from PXA250 will not be synchronized with its SDCLK clock.

- Because of a mismatch between the required time interval for asserting and dis-asserting Coral’s DREQ signal, as mentioned above, it is not possible to use DMA. The data transfer should take place without the DMA.

Please refer to the next page for the timing diagram.

4 Timing Diagram

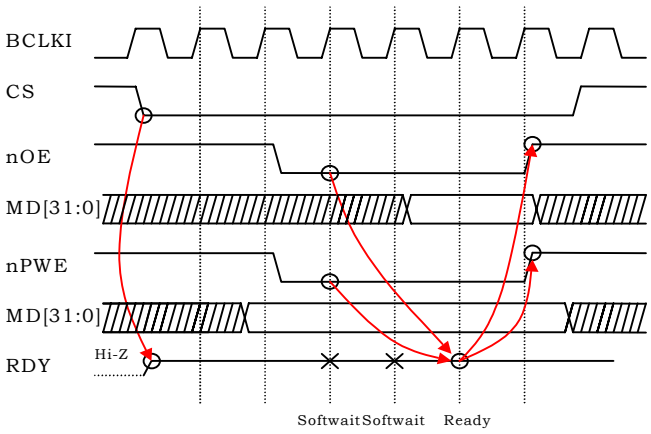

Fig 3. No Hardware wait

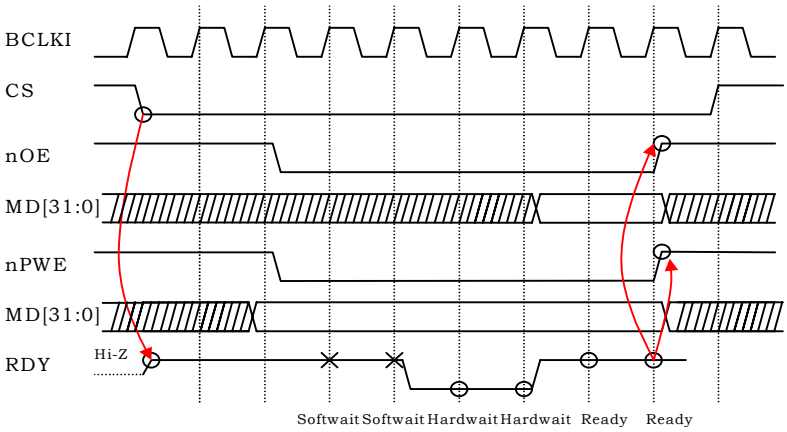

Fig 4. Hardware wait