GRAPHICS CONTROLLERS
MB88F33X INDIGO2(-X)

APIX2 COMPLIANCE TEST
REV0.1
APPLICATION NOTE
<table>
<thead>
<tr>
<th>Rev</th>
<th>Date</th>
<th>Author</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.1</td>
<td>2013-11-21</td>
<td>AP</td>
<td>initial</td>
</tr>
</tbody>
</table>
Warranty and Disclaimer

The use of the deliverables (e.g. software, application examples, target boards, evaluation boards, starter kits, schematics, engineering samples of IC’s etc.) is subject to the conditions of Fujitsu Semiconductor Europe GmbH (“FSEU”) as set out in (i) the terms of the License Agreement and/or the Sale and Purchase Agreement under which agreements the Product has been delivered, (ii) the technical descriptions and (iii) all accompanying written materials.

Please note that the deliverables are intended for and must only be used for reference in an evaluation laboratory environment.

The software deliverables are provided on an as-is basis without charge and are subject to alterations. It is the user’s obligation to fully test the software in its environment and to ensure proper functionality, qualification and compliance with component specifications.

Regarding hardware deliverables, FSEU warrants that they will be free from defects in material and workmanship under use and service as specified in the accompanying written materials for a duration of 1 year from the date of receipt by the customer.

Should a hardware deliverable turn out to be defect, FSEU’s entire liability and the customer’s exclusive remedy shall be, at FSEU’s sole discretion, either return of the purchase price and the license fee, or replacement of the hardware deliverable or parts thereof, if the deliverable is returned to FSEU in original packing and without further defects resulting from the customer’s use or the transport. However, this warranty is excluded if the defect has resulted from an accident not attributable to FSEU, or abuse or misapplication attributable to the customer or any other third party not relating to FSEU or to unauthorised decompiling and/or reverse engineering and/or disassembling.

FSEU does not warrant that the deliverables do not infringe any third party intellectual property right (IPR). In the event that the deliverables infringe a third party IPR it is the sole responsibility of the customer to obtain necessary licenses to continue the usage of the deliverable.

In the event the software deliverables include the use of open source components, the provisions of the governing open source license agreement shall apply with respect to such software deliverables.

To the maximum extent permitted by applicable law FSEU disclaims all other warranties, whether express or implied, in particular, but not limited to, warranties of merchantability and fitness for a particular purpose for which the deliverables are not designated.

To the maximum extent permitted by applicable law, FSEU’s liability is restricted to intention and gross negligence. FSEU is not liable for consequential damages.

Should one of the above stipulations be or become invalid and/or unenforceable, the remaining stipulations shall stay in full effect.

The contents of this document are subject to change without a prior notice, thus contact FSEU about the latest one.

Should one of the above stipulations be or become invalid and/or unenforceable, the remaining stipulations shall stay in full effect.
Contents

1 INTRODUCTION .............................................................................................................. 5

2 RX DOWNSTREAM JITTER ACCEPTANCE .................................................................. 6
   2.1 Measurement Equipment ...................................................................................... 6
   2.2 Calibration ........................................................................................................... 6
   2.3 Compliance Test .................................................................................................. 7
      2.3.1 MB88F33x ‘Indigo2(-x)’ Pattern Checker ................................................... 8
   2.4 Result ..................................................................................................................... 8

3 APPENDIX ..................................................................................................................... 10
   3.1 References ............................................................................................................ 10
1 Introduction

This document describes the setup and execution of the APIX2 compliance test for the Fujitsu Graphics Controllers. Reference for the compliance test is the application note from Inova Semiconductors [1]. This reference document describes the general measurement techniques and gives the compliance limits, whereas this application note covers the concrete realization with the Fujitsu graphics controllers.

This initial version covers the Rx downstream jitter acceptance compliance test for the MB88F33x ‘Indigo2(-x)’.
2 Rx Downstream Jitter Acceptance

The compliance document specifies two measurement approaches. The test method described in this chapter is the single tone approach with cable generated ISI as it is applied to the compliance test of the Fujitsu graphics controllers.

2.1 Measurement Equipment

The jitter acceptance measurement requires following measurement equipment:

- **Pattern generator**
  - Frequency min 3 GHz
  - Delay control input
  - Optional: Jitter generation option (RJ, ISI)
  - Used at Fujitsu: Agilent 81143A

- **Function generator**
  - Frequency min 50 MHz
  - Used at Fujitsu: Agilent 81160A

- **Oscilloscope (for calibration)**
  - Bandwidth min 6 GHz
  - Sample Rate min 20GS/s
  - Jitter analysis option
  - Used at Fujitsu: LeCroy SDA 808Zi-A

- **Cable**
  - LEONI Dacar 535 with different lengths

- **Rosenberger HSD SMA interface (test fixture)**

2.2 Calibration

The calibration routine measures the jitter components which correspond to the amplitude of the jitter signal. Since random jitter and ISI do not change, the relevant component is the periodic jitter PJ.

- **Pattern generator setup**
  - Enable selected bandwidth mode
  - Enable PRBS mode with 12 bit PRBS

- **If pattern generator is not able to generate ISI**
  - use test cable which generates about 235 mUI ISI, find suitable cable length
  - Set minimum amplitude that eye mask is not hit
  - Fujitsu: 4m LEONI Dacar 535 generates 220 mUI ISI for the 3 Gbps mode.

- **Scope setup**
  - Disable PLL for clock recovery, use constant clock

- **Increase jitter amplitudes (i.e. amplitude of function generator) and measure jitter (all components) for jitter frequencies according to Inova compliance document.**
Result is the dependency of the PJ on the jitter amplitude as shown in Figure 1 for the 3 Gbps mode.

![Jitter Acceptance Calibration](image)

Figure 1: Calibration result

The delay control input of the used pattern generator is limited. It is not possible to generate more than 700ps (i.e. 2.2 UI for the 3 Gbps mode) periodic jitter.

### 2.3 Compliance Test

The general measurement procedure is described in the compliance specification [1]. The following steps describe the procedure more detailed.

1. Setup pattern generator as described in step calibration
2. Set APIX RX configuration register for selected bandwidth mode
3. Set up Fujitsu pattern checker or alternative the Inova pattern checker (not described here)
4. Set initial jitter frequency
5. Set initial jitter amplitude
6. Increase jitter frequency
7. Increase jitter amplitude
   - errors occur? (observe status register)
   - no
   - Max. jitter frequency achieved
   - yes
   - stop pattern checker, clear status
   - save current value of jitter amplitude

![Compliance procedure](image)

Figure 2: Compliance procedure
2.3.1 MB88F33x 'Indigo2(-x)' Pattern Checker

Pattern Checker Setup:

<table>
<thead>
<tr>
<th>Address</th>
<th>Value</th>
<th>Module</th>
<th>Register name</th>
</tr>
</thead>
<tbody>
<tr>
<td>w 0x00020100</td>
<td>0x00000031</td>
<td>#mId:APIX2_PHY#</td>
<td>#rId:BIST_PATTGEN_LINK#</td>
</tr>
<tr>
<td>w 0x00020104</td>
<td>0x00000000</td>
<td>#mId:APIX2_PHY#</td>
<td>#rId:BistTestDuration#</td>
</tr>
<tr>
<td>w 0x0002010C</td>
<td>0x00000990</td>
<td>#mId:APIX2_PHY#</td>
<td>#rId:BistChkPrbsCfg#</td>
</tr>
<tr>
<td>w 0x00020110</td>
<td>0x00000004</td>
<td>#mId:APIX2_PHY#</td>
<td>#rId:BistCtrl#</td>
</tr>
</tbody>
</table>

Register description:

<table>
<thead>
<tr>
<th>Register</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>BIST_PATTGEN_LINK</td>
<td>0x31</td>
<td>Enable pattern checker and 3 Gbps mode</td>
</tr>
<tr>
<td>BistTestDuration</td>
<td>0x0</td>
<td>Run checker continuously</td>
</tr>
<tr>
<td>BistChkPrbsCfg</td>
<td>0x990</td>
<td>PRBS polynomial corresponding to Agilent pattern generator</td>
</tr>
<tr>
<td>BistCtrl</td>
<td>0x4</td>
<td>Initial status clear</td>
</tr>
<tr>
<td>BistCtrl</td>
<td>0x1</td>
<td>Start pattern checker</td>
</tr>
</tbody>
</table>

Table 1: MB88F33x 'Indigo2(-x)' pattern checker setup

Register to observe:

<table>
<thead>
<tr>
<th>Register</th>
<th>Address</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>BistDownStatus</td>
<td>0x00020114</td>
<td>Status of pattern checker</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Observe field Bist_Down_Err_Cnt</td>
</tr>
</tbody>
</table>

Table 2: MB88F33x 'Indigo2(-x)' pattern checker status register

2.4 Result

The measurement gives a curve as shown in Figure 3. The diagram shows only the periodic jitter, since the other jitter components are constant. The minimum should be slightly above the CDR bandwidth (9MHz for the 3Gbps bandwidth). Low frequency jitter below the CDR bandwidth is tracked by the PLL. The applied jitter increases for decreasing jitter frequencies.

The jitter acceptance is the minimum of the measured curve and must be higher than the limit mentioned in the compliance document to meet the compliance test.
Figure 3: Jitter acceptance measurement results
3 Appendix

3.1 References

[1] APIX2 Physical Layer Compliance, Inova Application Note AN204 Rev. 1.2