Reality Check: Challenges of mixed-signal VLSI design for high-speed optical communications
Mixed-signal VLSI for 100G and beyond

- 100G optical transport system
- Why single-chip CMOS?
- So what is so difficult?
- CHAIS ADC
- On-chip noise coupling
- Package and PCB design
- Testing issues
- Future challenges
100G Optical Transport system

To system (Router)
100G client module for
* 100G Ethernet or
* OTU-4
or 10 * 10G client module

To network
100G Coherent Receiver ADC DSP
10G MUX
Precoding

Optical Module
Optical -> Electrical
112 Gbps

Electrical -> Optical
10 * 11.1 Gbps

OTU-4

100G MUX
10 to 4 MUX

Framer / FEC

OTU-4

SFI-S / MLD / XFI
SFI-S
SFI-S
SFI-S
SFI-S
Why single-chip CMOS for 100G?

- **Massive data bandwidth between ADC/DAC and digital**
  - 4-channel 8b 56Gs/s ADC/DAC means 1.8Tb/s of data at interface
  - Getting this from one chip to another costs power and chip area
    - 10G SERDES link ~250mW/channel $\Rightarrow$ ~10W per ADC or DAC

- **Critical performance factor is power efficiency, not just speed**
  - Discrete ADC/DAC (e.g. SiGe) dissipating ~20W each (including I/O) are difficult to use
    - Very high total power dissipation in package (>100W for multiple channels)
    - Skew management/calibration problem (especially over temperature/lifetime)

- **Single-chip CMOS solution is the “Holy Grail”**
  - Integrate on ASIC with >50M gates or memory (size limited by power dissipation)
  - Leverage CMOS technology advances to drive down power and cost
  - ADC and DAC get faster and lower power at the same rate as digital -- hopefully 😊
ADCDSP -- so what is so difficult?

- **ADC is the biggest circuit design problem**
  - Ultra-high speed, low noise and jitter, low power consumption – all at the same time…
  - Conventional techniques cannot easily deliver required performance

- **Digital-analogue noise coupling**
  - Sampler/clock jitter ~100fs on same chip as DSP with >100A current spikes

- **Wide bandwidth (>20GHz) and good S11 (up to >30GHz)**
  - Sampler, package, PCB design all very challenging with high pin count FCBGA

- **On-chip DSP design is very out-of-the-ordinary (multiple TeraOPS)**
  - Extremely power-efficient ➔ use massive parallelism, not GHz clocks (Pentium 4…)

- **Test**
  - Performance verification challenges limits of test equipment
  - Need at-speed performance verification in production, not just functional testing
The ADC problem

- **Wideband low-noise sampler + demultiplexer + interleaved ADC array**
  - Smaller CMOS geometries ➔ higher speed ➔ worse mismatch and noise

- **Single 56Gs/s track/hold very difficult due to extreme speed**
  - <9ps to acquire, <9ps to transfer to following interleaved T/H stages

- **Interleaved track/hold (e.g. 4-channel 14Gs/s) also very difficult**
  - Signal/clock delays must match to <<1ps – how do you measure this?

- **Noise, mismatch and power of cascaded circuits all adds up**
  - Multiple sampling capacitors, buffers, switches, demultiplexers…

- **Layout and interconnect extremely challenging**
  - Design the circuits, then find you can’t actually connect everything up…

- **Interleaved ADC back-end is not so difficult (only in comparison!)**
  - Design for best power and area efficiency rather than highest speed
  - Interleave as many as necessary to achieve required sampling rate
  - 8 x 175Ms/s 8b SAR ADCs fit underneath 1 solder bump ➔ 45Gs/s per sq mm 😊
A 56Gs/s CMOS ADC solution – CHArge-mode Interleaved Sampler (CHAIS)

14GHz VCO (1 per ADC pair)

Clocks

4 Phase Sampler

Trim Voltages

Calibration

DEMUXA DEMUXB DEMUXC DEMUXD

ADCBANKA ADCBANKB ADCBANKC ADCBANKD

80 80 80 80

80 x ADC Inputs

80 x 8b ADC Outputs

DEMUX

Digital

Output

1024b

437.5MHz

Input
Dual ADC layout (4mm x 4mm test chip)
Example of 100G coherent receiver ASIC

- **Architecture:** Single CMOS die
- **Technology:** 65nm CMOS
- **Interconnect:** 12 layer metal
- **Die size:** 15 mm x 15 mm
- **Gate count:** ~50 million gates
- **Package:** FCBGA, >1000 pins
- **M/S macros:** 4 channel 56 Gs/s ADC
  24 channel CEI-11G TX
- **ADC power:** ~2W/channel
The DSP problem

- Digital design tools (and designers) *really* don’t like this type of DSP
  - The tools (and designers) synthesize circuits, then worry about how to connect them up
    - But interconnect capacitance causes ~90% of power dissipation, not circuits
  - Massive data bus widths (4k bits at ADC outputs) ➔ massive interconnect problem

- Partitioning into usable size blocks may be more difficult than it appears
  - Tools don’t like doing flat designs with tens of millions of gates (turn-around time)
    - “OK, lets split that big DSP block into two and add some pipelining”
    - “Erm, about this 16k bit wide data bus you’ve just introduced…” 😞

- Better system/architecture tools for this type of design are needed
  - Should really design/optimise the data flow, then shovel the circuits in underneath…
    - Designers’ brains (and system-level design tools) don’t really think this way 😞
On-chip noise coupling

- **Reduce aggressor (DSP logic) noise generation**
  - Use intentional skew of clock timing within each block and between blocks
    - Reduces peak current and spreads out in time ➔ >10x lower di/dt
  - Lots of on-chip (~400nF) and ultra-low-inductance (~4pH) in-package decoupling

- **Increase victim (ADC analogue) immunity**
  - Fewest possible noise/jitter sensitive circuits, all fully differential
  - Lots of on-chip (~100nF) and low-inductance in-package decoupling

- **Improve victim-aggressor isolation**
  - Avoid low-resistance epi substrate (short-circuit for substrate noise)
  - Build “nested walls” of isolation with most sensitive circuits in the middle
    - SAR ADCs (not jitter-sensitive) form the first line of defense
    - Isolation walls through package and into chip form the next line
    - Demux and other analogue circuits (calibration etc.) form the next line
    - Sampler and PLL are hidden away inside all these layers of isolation

- **Measurements show very little noise makes it past all the defenses 😊**
Package and PCB design

- **1mm pitch FCBGA, >1000 pins, 19 internal layers, copper lid**
  - Use similar package for test chips as typical ASIC to get same performance
  - Low-loss high-TCE LTCC (12ppm/C) for improved second-level reliability

- **Multiple power/ground regions and shields for noise isolation**

- **Ultra-low-inductance internal decoupling for supplies and bias/reference**
  - Multiple interleaved VDD/VSS planes connect chip to multi-terminal decouplers
  - Noise dealt with inside package \(\Rightarrow\) predictable (stops end user getting it wrong)

- **Coaxial via and waveguide structures, <1dB loss at 20GHz**
  - Ground planes completely removed above signal balls to reduce capacitance
  - Dual 100ohm balanced lines used to connect coaxial via structure to G-S-G pads

- **Optimized launch to G-S-G coplanar waveguide on low-loss PCB**
  - Balls on row inside signal pins removed to reduce capacitance, grounds cut back
  - Outer PCB layers use MEW Megtron 6 (very low loss, lead-free multilayer compatible)
Package + PCB EM field simulations
BATBOARD and ROBIN
Bandwidth measurement using TDR step

- Agilent DCA-J 86100C
- HP8665B Signal Generator
- 1.75GHz Differential Reference Clock
- Picosecond Pulse Labs TDR heads <10ps risetime
- Colby Instruments delay line with 1ps resolution
- Model 4022 TDR/TDT Source
- Model 4020RPH-RP head
- Model 4020RPH-RN head
- ADC_INP
- ADC_INM
- REFCLK
- BATBOARD
- SPI Interface
- PC running MATLAB
- 1.75GHz Differential Reference Clock
Frequency Response (test setup and ADC)

- Frequency response of test setup
  - TDR step (measured)
  - Batboard PCB (measured)
    - ENIG not Ag finish (Ni is lossy!)
    - Socket (estimated -1dB @ 20 GHz)

- Test setup loss similar to ADC response

- Corrected ADC frequency response
  - accurate measurements are not easy

- ADC -3dB bandwidth ~ 15GHz
  - very close to simulation and specification
Production test

- Need proper performance verification, not just functionality
  - Increased confidence that chip actually meets design specifications
  - Make chip self-testing as far as possible and do at-speed performance tests

- Drive ADC inputs from wideband n-way power combiners
  - Sum outputs of multiple CEI-11G channels with sinewave input(s)
  - Enable and disable channels/clocks instead of switching (avoid 20GHz+ relays)

- Test ADC ENOB using sinewave input(s)
  - Sampled data stored in on-chip RAMs then read out and analysed (ENOB)
  - Signal source TBD (filtered DRO? phase locked to REF?) – high quality essential

- Test CEI-11G outputs by looping back into 56Gs/s ADC inputs
  - 5 samples per bit gives complete waveform analysis on *all* TX channels
  - Full-speed measurement of eye opening and jitter
Future challenges -- what obstacles are there to progress beyond 100Gb/s?

- **Sampler noise/bandwidth/interleave skew/clock jitter**
  - Can be solved using new CMOS techniques instead of exotic technology
    - CHAIS sampler/demux/ADC is capable of >100Gs/s even in 65nm
    - Bandwidth scales with clock rate (-3dB at ~0.3Fs)

- **Input bandwidth increase and S11 improvement**
  - FBGA package modifications to optimize design for very high frequencies
    - Smaller ball pitch conflicts with second-level reliability and PCB issues

- **Power consumption – DSP issue, ADC is ~2W/channel (65nm, scales like digital)**
  - DSP power is several times ADC power, especially with more complex systems
    - Power increase (complexity) is outrunning power savings (process shrink)

- **Layout (interconnect and floorplan) feasibility**
  - Everything wants to be on top of everything else with zero-length connections 😐
    - Could need unconventional layouts – ADCs might look like dartboards 😊
THE POSSIBILITIES ARE INFINITE