

MB86061

12-Bit 400MSa/s Digital to Analog Converter

FME/MS/SFDAC1E/FL_1/4269

The Fujitsu MB86061 is a high performance 12-bit 400MSa/s digital to analog converter (DAC). Use of novel techniques for the converter architecture delivers high speed operation consistent with BiCMOS or bipolar devices but at the low power of CMOS. Fujitsu's proprietary architecture is the subject of several patent applications. Excellent SFDR performance coupled with high speed conversion rate and low power make this device particularly suitable for high performance communication systems, graphics and test/instrumentation equipment applications.

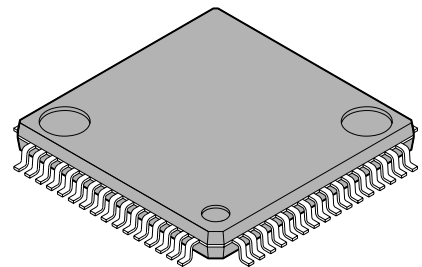
Features

- 12-bit 400MSa/s Digital to Analog converter
- True ECL digital interface (-2V supply)
- 86dBc SFDR @ 10MHz, 200MSa/s (Shuffle On)
- Low power, +3.3V and -2V operation (308mW @ 300MSa/s)
- Performance enhanced pinout with on-chip decoupling
- 0.35µm CMOS technology with Triple Well
- Industrial temperature range (-40 °C / +85 °C)
- Plastic Package 64-pin QFP

Applications

- Test & Instrumentation equipment
- Communications systems
- High performance graphics

PLASTIC PACKAGE QFP-64



(FPT-64P-M09)

Ordering Information

Part	Order Number
MB86061 Datasheet	Contact Sales
MB86061 DAC	MB86061PFQ
MB86061 Development Kit	DK86061-3
MB86061 Development Kit User Manual	Contact Sales

This product has Patents applied for in the US and elsewhere including GB2333191A, EP0935345A, JP11-274934A, GB2333171A, EP0930717A, JP11-274935A, GB2333190A, EP0929158A, JP11-243339A, GB2335097A, EP0940923A, JP11-317667A, GB2335076A, EP0940852A, JP11-251530A.

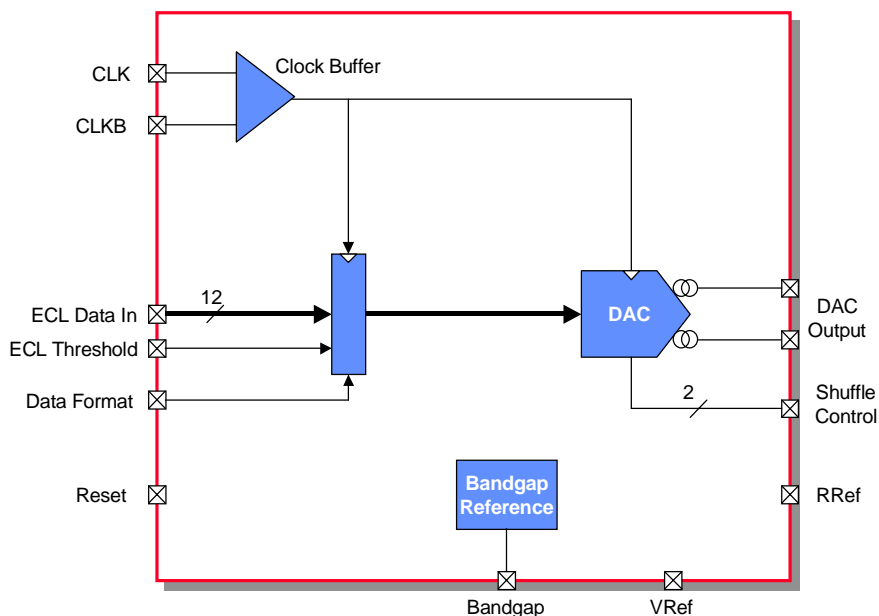
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Functional Description

The MB86061 is a high performance 12-bit 400MSa/s digital to analog converter. Versatile interfacing via the 12-bit true ECL data input allows existing system requirements to be accommodated, using either offset binary or 2's complement data formats. The device requires an external clock.

A 1.25V bandgap reference is provided on-chip, which may be overdriven where an external reference is to be used. A power-down mode is enabled during device reset, with the current output drive and reference circuitry disabled.

The device is manufactured in a 0.35 μ m advanced CMOS process with Triple Well extension giving improved isolation between analog blocks and digital-analog.



MB86061 Functional Block Diagram

Converter Architecture

The DAC core incorporates a number of novel design aspects that are subject to patent applications. Key to its operation are the current sources where segmented, common centroid, interleaved techniques for the most significant bits, as well as load matching ensure good linearity and low distortion to at least the 12-bit level. In the switch elements tracking capacitance is minimised to improve settling, while controlled rise and fall times improve SFDR performance. Finally the digital decoding uses a 3-dimensional addressing approach to minimise propagation delays from latch to element.

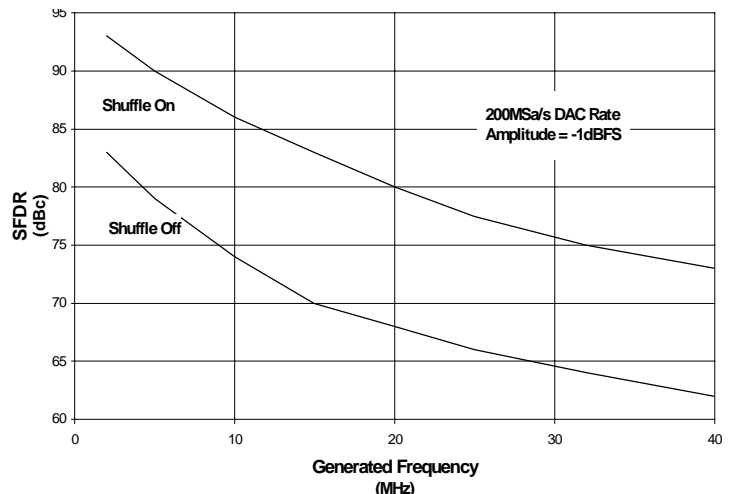
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Segment Shuffling

The DAC core incorporates a proprietary segment shuffling capability which is provided to further improve linearity, and hence improve SFDR. This feature reduces any signal level dependent effects on linearity as the same code can be generated by the same number of MSB cells but taken from any quarter of the MSB segments. Segment shuffling can be selected to operate every 4, 8 or 16 updates of the DAC output using a random shuffle sequence between the four segments.

The effect of segment shuffling is to produce a spread noise spectrum, raising the overall noise floor, but reducing the distortion. For minimum distortion when generating low frequency signals, it is recommended that the shuffling clock rate is no more than 25MHz (DAC Rate / Segment Shuffling Setting). However, low shuffle clock rates give reduced spreading out of distortion components.

Single Tone SFDR Performance



Spurious Free Dynamic Range (SFDR)

Spurious Free Dynamic Range (SFDR) is defined as the highest spurious product (harmonic or non-harmonically related) within a defined bandwidth while generating a test tone or tones. SFDR varies with amplitude and frequency of the test tone(s) and is either quoted as the difference between the tone and highest spurious component (dBc) or referenced to full scale (dBFS). The measurement bandwidth is typically regarded as DC to Nyquist but occasionally systems will specify an appropriate narrow band.

Development Kit

A development kit, reference DK86061, is available for the MB86061 12-Bit 400MSa/s Digital to Analog Converter. The kit includes an evaluation board that enables simple and effective evaluation of the device.

The board provides a complete evaluation environment for the DAC. A transformer coupled differential output interface is provided to simplify integration into target applications and development environments. An RF clock source can be connected via the transformer coupled input, and 12-bit data via a 40-way IDC header.

The development kit includes,

- Evaluation board with MB86061 device fitted
- Spare MB86061 for customer development
- User Manual



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