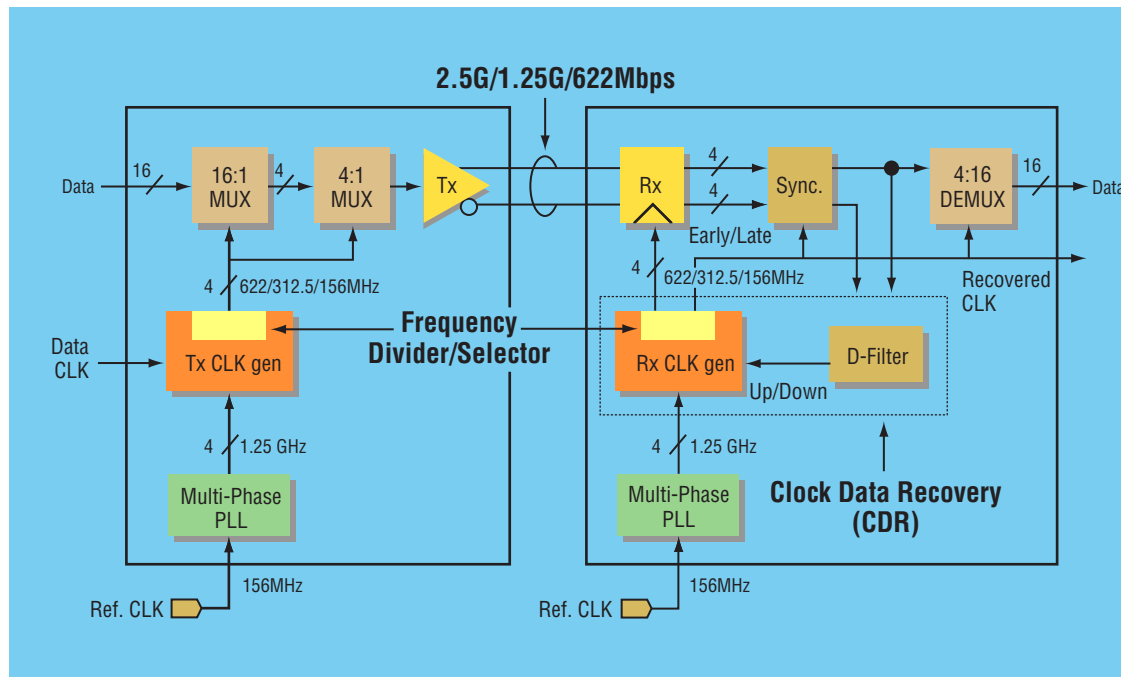


# 2.5Gbps Transceiver Macro with CDR



## Features

- CMOS 0.18 micron technology
- 16-bit parallel transmitter and receiver arrays, other bit width also available
- Field programmable triple mode input data rate, 2.5Gbps, 1.25Gbps, and 622Mbps
- Differential PCML transmitter ( $V_{tt}=1.8V$ )
- Equalized receiver obviating the need for pre-emphasis thereby reducing power dissipation
- 156MHz input reference clock
- Individual bit clock phase recovery using CDR (Clock Data Recovery)
- Complies with SONET/SDH jitter tolerance mask
- Integrated on-chip 50 ohm termination resistor on transmitter and receiver
- Field programmable transmitter output current control enabling optimum power consumption per application
- Low power < 2.5W for 16-bit transmitter array and 16-bit receiver array (typical)

## Benefits

- Available as core library cell for ASIC design
- Low power dissipation
- Dual 1.8V/3.3V supply
- Individual application programmability

# 2.5Gbps Transceiver Macro with CDR

## ► Description

Fujitsu's triple mode parallel transceiver is a physical I/O interface macro for ASICs that performs high-speed back plane data communication, operating at low power dissipation. The triple data transfer rates, 2.5G/1.25G/622M bps, can be selected depending on the system requirements. The macro consists of a 16-bit transmitter, and a 16-bit receiver array. The receiver macro contains CDR (Clock Data Recovery) using dual loop PLL (analog and digital PLL), that complies with SONET/SDH jitter tolerance mask, up to 72-bit run length. The Receiver has an integrated line equalization capability to compensate for inter-symbol-interference (ISI), which enables a wide variation in data link length and range, from short PCB trace to long twisted pair cables connections. The device also includes on-chip PRBS generators and comparators for testability.

## ► Deliverables

Fujitsu's 2.5Gbps Transceiver Macro enables customers to design a variety of complex system-on-a-chip ASIC designs for high-end networking applications.

A Fujitsu application engineer works with the customer to identify the customers' specific IP requirements. Fujitsu will provide the customer with the following information to support the 2.5Gbps Transceiver macro:

The macro is fabricated using Fujitsu's advanced 0.18 $\mu$ m CMOS technology with supply voltage of 1.8V and 3.3V. It can be used with a variety of packages, such as EBGA and FCBGA.

This macro can be used in a variety of applications:

- Wavelength Division Multiplex (WDM) equipment
- Section repeaters
- Add Drop Multiplexers (ADM)
- Broadband cross-connects
- Fiber optic terminators
- Fiber optic test equipment

- Verilog Model
  - Front-end simulation
  - C model with Verilog wrapper
- Design Compiler Model
  - Timing analysis
  - Place and Route
- Library Exchange Format (LEF)
  - Floor planning

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