

Mixed Signal Division

MB86628

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Version 1.0

FME/MS/QUADAFE/FL_1/4635

KeyWave™ II Quad AFE

The Fujitsu MB86628 KeyWave™ II Quad AFE incorporates four complete analog front ends, optimised for Central Office (CO) ADSL modems. The device integrates high resolution analog to digital converters (ADC) and digital to analog converters (DAC), which combined with active filtering significantly reduces the requirements placed on external components. The MB86628 KeyWave™ II Quad AFE is ideal for cost, power and board area sensitive CO equipment.

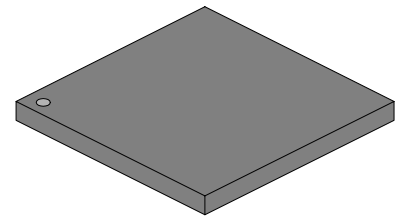
Features

- Integrates four complete full-rate ADSL analog front ends
- Integrates all active circuits except transmit line drivers
- Low power, 3.3V operation
 - 235 mW/port (G.dmt)
 - 200 mW/port (G.lite)
- Integrated analog filters and 15-bit A/D & D/A converters
- Interpolation filtering to reduce transmit channel data rate
- 0 to +48 dB PGA range for each receive channel
- Excellent SFDR and input noise performance
- 0.35µm CMOS technology with Triple Well
- Industrial temperature range (-40 °C to +85 °C)

Applications

- High port-density Central Office ADSL modem systems
- Programmable for ADSL derivatives (e.g. G.lite, splitterless, Universal ADSL)
- Compatible with FDM and echo cancelling systems
- Supports ADSL over ISDN

PLASTIC PACKAGE EFBGA-216



Ordering Information

Part	Order Number
MB86628 Datasheet	Contact Sales
MB86628 KeyWave Quad AFE	MB86626PBT
MB86628 Development Kit	DK86628-1
MB86628 Development Kit User Manual	Contact Sales

Functional Description

Each of the four analog transmit and receive channels consists of a 15-bit DAC with associated anti-imaging filters, a 15-bit ADC with anti-aliasing filter and a programmable gain summing amplifier (PGA). All analog signal paths are differential. A clock multiplier and bandgap references are incorporated on-chip. A parallel data interface allows for high speed data transfer of the transmit/receive data, while a serial interface is provided for control and configuration. Integrated transmit interpolation filters reduce the data rate required to be provided by the modem, while maintaining the benefits of using a faster DAC update rate.

This highly integrated device reduces the number of components required for the line interface to a transmit line driver and a small number of passive components per port. A functional block diagram is shown in Figure 1.

The device is manufactured in a 0.35µm CMOS process using Fujitsu's Triple Well technology, giving excellent isolation between analog and digital-analog blocks.

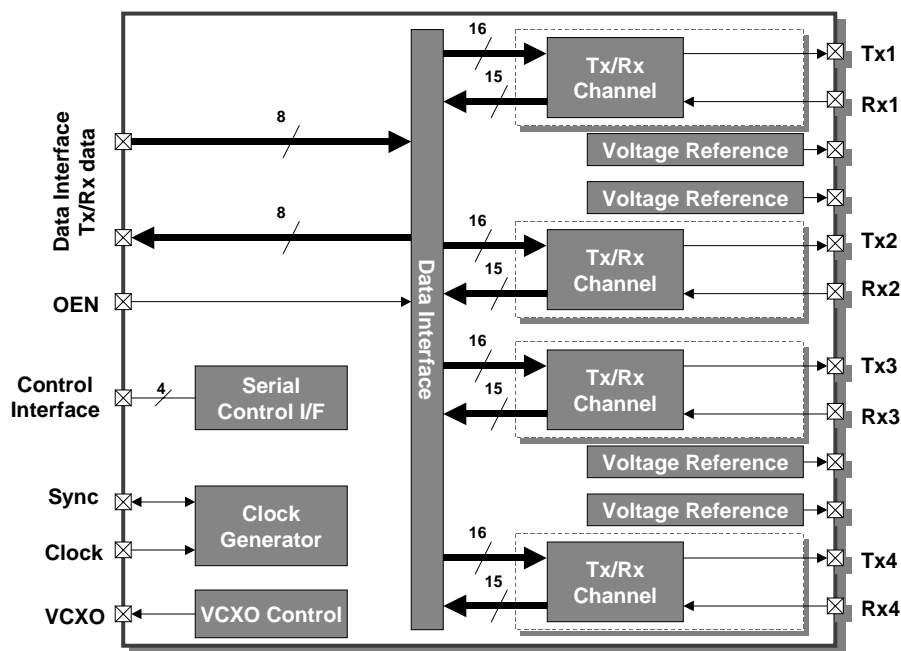


Figure 1 MB86628 Functional Block Diagram

MB86628 KeyWave™ II Quad AFE

Transmit and Receive Channels

Each receiver front end has constant resistance programmable attenuators to allow for variable line lengths, and to maintain sufficient dynamic range in the programmable gain low noise summing amplifier. Anti-aliasing filters are included which have programmable cut-off frequency and gain control. SNR can be improved by matching the line impedance with the use of the hybrid balance trim input which reduces echo signals at the input.

The attenuators, summing amplifier and filter give a total gain range from input to ADC of 0 to +48dB.

The transmit paths feature an interpolating filter to increase the DAC update rate without unnecessary loading on the modem by minimising data transfer over the parallel data interface. The anti-imaging filter can be programmed for both cut-off frequency and gain.

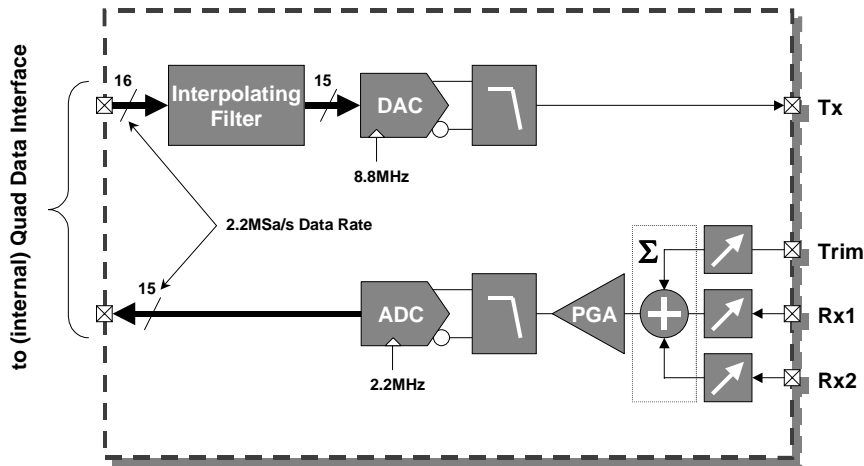


Figure 2 MB86628 Tx/Rx Channel Functional Block Diagram

The transmit and receive analog filters are programmable for both gain and frequency cut-off. Frequency cut-off is selectable between one of four settings, 150kHz, 300kHz, 600kHz and 1.2MHz, and with fifteen fine adjustment steps available in-between. Power control is provided to enable further power optimisation. In the receive path a distributed gain approach is implemented, split between filter and front end PGA & Summer. A high performance 15-bit 8.8 MHz DAC and 15-bit 2.2 MHz ADC convert DSL signals to and from the line in each transmit and receive channel.

Data and Serial Control Interfaces

Data is transferred to and from the device via a 2 x 8-bit unidirectional data interface. Two stage IIR digital filters are included which provide interpolation from 2.2MSa/s to 8.8MSa/s per channel in the Tx direction. In the Rx direction, the data rate is 2.2MSa/s. For both the Tx and Rx paths, the MSByte and LSByte of the 16bit words are interleaved at a data rate of 17.6 million bytes/second.

All four AFE channels have the same synchronization, referenced to a 2.2MSa/s SYNC pin, which may be defined either internal to the device (SYNC output) or externally (SYNC input). An output enable pin, OEN, may be used to tristate the ADC data pins, if required.

A 4-wire serial interface is provided for the downloading of control and configuration information to the device. The registers are 16-bit wide, and are individually accessed using an 8-bit address and control word. All registers support read and write access.

Registers for transmit and receive control are duplicated four times, once for each AFE channel, while other system level configuration registers (e.g. Clock Multiplier registers etc.) are global.

Clock Multiplier

The device requires a clock source which may be an external reference, or a VCXO which can be locked to the line symbol rate. The clock generator takes a low-jitter 17.6MHz clock, and generates an 88MHz clock used for internal clocking as well as a differential output clock.

VCXO Control

The integral VCXO control provides an effective means of controlling an external VCXO clock source. This digital output uses a first order sigma-delta DAC, programmed from a 20-bit register. External RC filtering would normally be provided.

Voltage Reference

Four internal bandgap references are provided. These can be bypassed in applications where suitable external references are available.

MB86628 KeyWave™ II Quad AFE

Development Kit

A development kit, reference DK86628-1, is available for the MB86628 KeyWave™ II Quad AFE. The kit includes an evaluation board that enables simple and effective evaluation of the device.

Please contact your Fujitsu representative for further information.

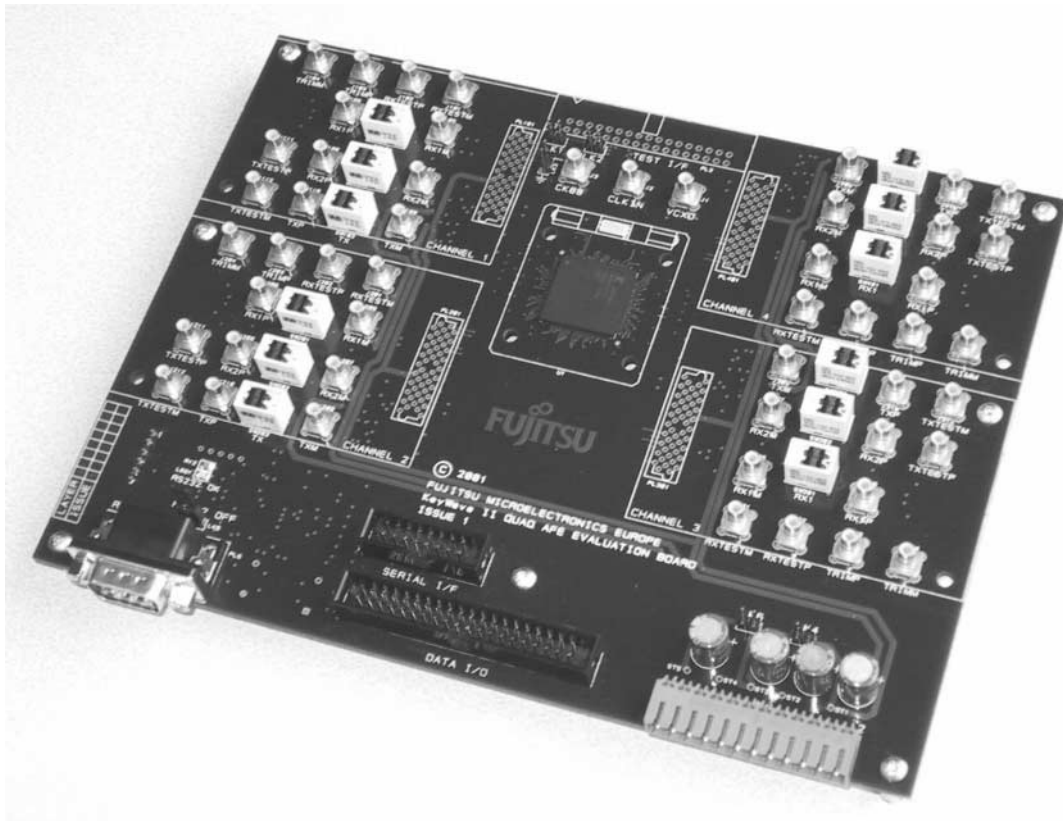


Figure 3 DK86628-1Quad AFE Development Kit

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