



F²MC-16 Family
16-bit Microcontroller
SOFTUNE Assembler Additional Manual

1. List of Added Options

The added start-up options are listed in **Table 1**.

■ List of Added Options

Table 1 List of Added Options

Format	Function outline	Initial value
Target-dependent option		
-div905	Does not replace <i>DIV/DIVW</i> instruction with alternative instruction	Does not replace
-xdiv905	Replaces <i>DIV/DIVW</i> instruction with alternative instruction	
-div_check	Does not issue warning message warning to <i>DIV/DIVW</i> instruction	Issues warning message
-xdiv_check	Issues warning message to <i>DIV/DIVW</i> instruction	

2. Details of Added Options

The added start-up options are explained.

■ Added Options

There are four added options as follows:

- `-div905` ······ Does not replace ***DIV/DIVW*** instruction with alternative instruction
- `-xdiv905` ······ Replaces ***DIV/DIVW*** instruction with alternative instruction
- `-div_check` ····· Does not issue warning message warning to ***DIV/DIVW*** instruction
- `-xdiv_check` ····· Issues warning message to ***DIV/DIVW*** instruction

2.1 -div905 and -Xdiv905

These options relate to notes in the "DIV A,Ri" and "DIVW A,RWi" instructions of the MB90500 series.

The `-div905` option does not replace the *DIV/DIVW* instruction with an alternative instruction.

The `-xdiv905` option replaces the *DIV/DIVW* instruction with an alternative instruction.

These options are valid only for the F²MC-16 family (MB90500 series).

■ -div905

[Format]

```
-div905
```

[Explanation]

This option does not replace the *DIV/DIVW* instruction with an alternative instruction.

[Example]

```
fas907s -cpu mb90500 test -div905
```

<Caution>

-
- The `-div905` option is valid only for the F²MC-16 family (MB90500 series).
-

■ -xdiv905

[Format]

```
-xdiv905
```

[Explanation]

This option replaces the *DIV/DIVW* instruction with an alternative instruction.

[Example]

```
fas907s -cpu mb90500 test -div905 -xdiv905
```

<Caution>

-
- The `-xdiv905` option is valid only for the F²MC-16 family (MB90500 series).
-

■ Notes of Signed Division Instruction of F²MC-16LX CPU

- Devices

All devices (Eva, OTP, FLASH, Mask) of F²MC-16LX series.:

MB90520/A, MB90540, MB90550A, MB90560, MB90570/A, MB90580/B, MB90590, MB90595,

All devices of QCM16LX core.

- Notes in use

Normally remainder of the execution result of the signed division instruction ("DIV A,Ri" and "DIVW A,RWi") is set bank "00" area.

But above devices set remainder bank (DTB/ADB/USB/SSB) area.

When you use the signed division instruction, remainder is set at a bank area of the DTB/ADB/USB/SSB registers value.

Details are shown as follows.

• Notes in use of "DIV A,Ri" and "DIVW A,RWi" instructions

The remainder of the execution result of the signed division instruction ("DIV A,Ri" and "DIVW A,RWi") is stored in the address (bit0-15) which corresponds to the register of the instruction operand of bank area (bit16-23) according to an undermentioned table.

Therefore, please adjust the corresponding bank register to "00" and use the "DIV A,Ri" and "DIVW A,RWi" instructions.

Instruction	Bank Register	Address where the remainder is stored
DIV A, R0	DTB	(DTB:bit16-23)+(0180h+RP×10h+8h:bit0-15)
DIV A, R1		(DTB:bit16-23)+(0180h+RP×10h+9h:bit0-15)
DIV A, R4		(DTB:bit16-23)+(0180h+RP×10h+Ch:bit0-15)
DIV A, R5		(DTB:bit16-23)+(0180h+RP×10h+Dh:bit0-15)
DIVW A, RW0		(DTB:bit16-23)+(0180h+RP×10h+0h:bit0-15)
DIVW A, RW1		(DTB:bit16-23)+(0180h+RP×10h+2h:bit0-15)
DIVW A, RW4		(DTB:bit16-23)+(0180h+RP×10h+8h:bit0-15)
DIVW A, RW5		(DTB:bit16-23)+(0180h+RP×10h+Ah:bit0-15)
DIV A, R2	ADB	(ADB:bit16-23)+(0180h+RP×10h+Ah:bit0-15)
DIV A, R6		(ADB:bit16-23)+(0180h+RP×10h+Eh:bit0-15)
DIVW A, RW2		(ADB:bit16-23)+(0180h+RP×10h+4h:bit0-15)
DIVW A, RW6		(ADB:bit16-23)+(0180h+RP×10h+Ch:bit0-15)
DIV A, R3	USB *1	(USB *2:bit16-23)+(0180h+RP×10h+Bh:bit0-15)
DIV A, R7	SSB *1	(USB *2:bit16-23)+(0180h+RP×10h+Fh:bit0-15)
DIVW A, RW3		(USB *2:bit16-23)+(0180h+RP×10h+6h:bit0-15)
DIVW A, RW7		(USB *2:bit16-23)+(0180h+RP×10h+Eh:bit0-15)

*1 select by S bit of CCR register

*2 S bit of CCR register is 0

When the value of the bank register is "00", the remainder is stored in the register of the instruction operand. However, the remainder is stored in bank (DTB/ADB/USB/SSB) area, except when the value of the bank register is "00".

[Example]

Case of DTB = 053H and RP = 003H

Address of R0 is $00180H + 003H \times 010H + 08H = 0001B8H$. Bank register which used "DIV A,R0" is DTB which address is 053H.

Therefore, the remainder of the execution result of "DIV A,R0" is preserved in memory which address is 05301B8H.

(Please refer to the explanation of the general register of the manual for Ri and RWi.)

- About avoiding the Notes

Please use this compiler and the assembler when you use the MB905XX series because the one that the function to replace the signed division instruction with an equivalent instructions was added will be changed in the compiler so as not to generate the signed division instruction to have the program evade the Notes and developed and be offered in the assembler as follows.

The kind which will be developed in the future will improve the Notes as MB904XX series.

Measures assembler : asm907a V03L04 or later

fasm907s V30L04(Rev.300004) or later

Measures compiler : cc907 V02L06 or later

fcc907s V30L02 or later

Moreover, this Notes can be avoided by having use in the F²MC-16L mode in a present compiler.

- Supplementation explanation

• About the influence on the program which has developed Notes

The Notes can be confirmed which the operation by Eva-device on a system. Therefore, the problem does not occur if a normal operation is confirmed in debugging though there is the signed division instruction in the program.

In the program development by the assembler:

- (1) There is no problem if "DIV A,Ri" and "DIVW A,RWi" are not used.
- (2) There is no problem if each bank register is "00" though "DIV A,Ri" and "DIVW A,RWi" are used.
- (3) The DIV instructions excluding this does not have the problem.

In the program development by C compiler:

- (1) In small model and medium model, there is no problem when the bank register which __far type qualified data and nor corresponds is used by "00"(initial value).
(In small model and medium model, C compiler does not change the value of each bank register initialized by the startup routine when there is no __far type qualified data.)
- (2) There is a possibility that "DIV A,R2", "DIV A,R6", "DIVW A,RW2", and the "DIVW A,RW6" instructions are influenced for either by ADB as follows even if the corresponding bank register is used by "00h"(initial value).
 - In small model and medium model, there is __far type qualified data.
 - Compact model and large model are used.

(C compiler has the possibility to change the ADB register for the condition of (2))

However, there is no problem in the program if a normal operation is confirmed in debugging.

2.2 -div_check and -xdiv_check

These options relate to notes in the "DIV A,Ri" and "DIVW A,RWi" instructions of the MB90500 series.

The `-div_check` option issues a warning message to the *DIV/DIVW* instruction.

The `-xdiv_check` option does not issue a warning message to the *DIV/DIVW* instruction.

These options are valid only for the F²MC-16 family (MB90500 series).

■ -div_check

[Format]

```
-div_check
```

[Explanation]

This option issues a warning message to the *DIV/DIVW* instruction.

[Example]

```
fas907s -cpu mb90500 test -div_check
```

<Caution>

-
- The `-div_check` option is valid only for the F²MC-16 family (MB90500 series).
-

■ -xdiv_check

[Format]

```
-xdiv_check
```

[Explanation]

This option does not issue a warning message to the *DIV/DIVW* instruction.

[Example]

```
fas907s -cpu mb90500 test -div_check -xdiv_check
```

<Caution>

-
- The `-xdiv_check` option is valid only for the F²MC-16 family (MB90500 series).
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3. Added Error Message

The added error message is shown below.

■ Added Error Message

W1805A	Invalid instructions (DIV, DIVW) are detected
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[Program processing]

Continues processing