CM44-10105-4ET1

Errata

F²MC-16LX
16-BIT MICROCONTROLLER
MB90590 Series
HARDWARE MANUAL

2003.07.08

<table>
<tr><th>Page</th><th>Item</th><th>Description</th></tr>
<tr><td>14</td><td>1.8</td><td>The following terms were added to the summary of "1.8 Handling Device" as indicated by the shading below:

• Preventing latch-up
• Stabilization of supply voltage
• Treatment of unused pins
• Using external clock
• Power supply pins (Vcc/Vss)
• Pull-up/down resistors
• Crystal Oscillator Circuit
• Turning-on Sequence of Power Supply to A/D Converter and Analog Inputs
• Connection of Unused Pins of A/D Converter
• N.C. Pin
• Precautions at power on
• Initialization
• Indeterminate outputs from ports 0 and 1
• Using the "DIV A, Ri" and "DIVW A, RWi" instructions
• Using REALOS
• Notes on during operation of PLL clock mode

The following description was added to "■ Handling the Device":

❍ Stabilization of supply voltage
A sudden change in the supply voltage may cause the device to malfunction even within the specified Vcc supply voltage operating range. Therefore, the Vcc supply voltage should be stabilized.
For reference, the supply voltage should be controlled so that Vcc ripple variations (peak-to-peak values) at commercial frequencies (50 to 60Hz) fall below 10% of the standard Vcc supply voltage and the coefficient of fluctuation does not exceed 0.1 V/ms at instantaneous power switching.</td></tr>
<tr><td>76</td><td>5.2</td><td>The description in Table 5.2-2 was corrected as indicated by the shading below:

<table>
<tr><th rowspan="2">Type of reset</th><th colspan="5">CKSCR</th><th colspan="2">LPMCR</th></tr>
<tr><th>WS1</th><th>WS0</th><th>MCS</th><th>CS1</th><th>CS0</th><th>CG1</th><th>CG0</th></tr>
<tr><td>$\overline{HST}+\overline{RST}$</td><td>N</td><td>N</td><td>Y</td><td>N</td><td>N</td><td>Y</td><td>Y</td></tr>
</table>
</td></tr>
<tr><td>90</td><td>6.3</td><td>The description in Table 6.3-2 was corrected as indicated by the shading below:

Table 6.3–2 List of Instructions Used for Transition to Low-power Mode
<table>
<tr><td>MOV io,#imm8</td><td>MOV dir,#imm8</td><td>MOV eam,#imm8</td><td>MOV eam,Ri</td></tr>
<tr><td>MOV io,A</td><td>MOV dir,A</td><td>MOV addr16,A</td><td>MOV eam,A</td></tr>
<tr><td>MOV @RLi+dip8,A</td><td></td><td></td><td></td></tr>
<tr><td>MOVW io,#imm16</td><td>MOVW dir,#imm16</td><td>MOVW eam,#imm16</td><td>MOVW eam,RWi</td></tr>
<tr><td>MOVW io,A</td><td>MOVW dir,A</td><td>MOVW addr16,A</td><td>MOVW eam,A</td></tr>
<tr><td>MOVW @RLi+dip8,A</td><td></td><td></td><td></td></tr>
<tr><td>SETB io:bp</td><td>SETB dir:bp</td><td>SETB addr16:bp</td><td></td></tr>
<tr><td>CLRB io:bp</td><td>CLRB dir:bp</td><td>CLRB addr16:bp</td><td></td></tr>
</table>
</td></tr>
</table>

<table>
<tr><th>Page</th><th>Item</th><th>Description</th></tr>
<tr><td>182</td><td>14.3.3</td><td>The description " [bits 7 to 5] PCS2 to 0 (PPG count select): Count clock selection bit" of "■ PPG0, 1 Clock Select Register (PPG01)" was corrected as indicated by the shading below:

<table>
<tr><th>PCS2</th><th>PCS1</th><th>PCS0</th><th>Operation mode</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Peripheral clock (62.5 ns machine clock, 16 MHz)</td></tr>
<tr><td></td><td></td><td></td><td></td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Clock input from the timebase timer (128 µs, 4 MHz source oscillation)</td></tr>
</table></td></tr>
<tr><td>183</td><td></td><td>The description " [bits 4 to 2] PCM2 to 0 (PPG count mode): Count clock selection bit" of "■ PPG0, 1 Clock Select Register (PPG01)" was corrected as indicated by the shading below:

<table>
<tr><th>PCM2</th><th>PCM1</th><th>PCM0</th><th>Operation mode</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Peripheral clock (62.5 ns machine clock, 16 MHz)</td></tr>
<tr><td></td><td></td><td></td><td></td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Clock input from the timebase timer (128 µs, 4 MHz source oscillation)</td></tr>
</table></td></tr>
<tr><td>201</td><td>16.5</td><td>The description "❍ External interrupt request level" of "■ Notes on Using DTP/External Interrupts" was corrected as indicated by the shading below:

To detect an edge for an edge request level, the pulse width must be at least three machine cycles.
As shown in Figure 15.5-1 "Clearing the Interrupt Request Flag Bit (EIRR:ER) Upon Level Set", when the request input level is related to the level setting, a request that is input from an external device to the interrupt controller is kept active while the interrupt request is enable (ENIR:EN=1), even if the request is later canceled. To cancel the request to the interrupt controller, the interrupt request flag bit (EIRR:ER) must be cleared as shown in Figure 15.5-2 "Interrupt Cause and Interrupt Request to the Interrupt Controller While Interrupts are Enabled".

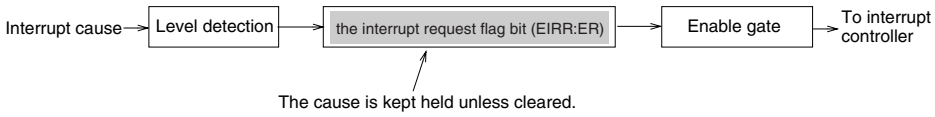
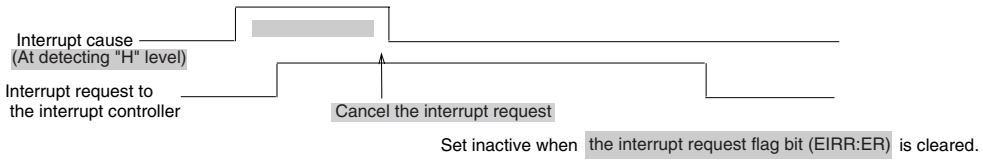
Figure 15.5-1 Clearing the Interrupt Request Flag Bit (EIRR:ER) Upon Level Set


Figure 15.5-2 Interrupt Cause and Interrupt Request to the Interrupt Controller While Interrupts are Enabled

</td></tr>
</table>

<table>
<tr><th>Page</th><th>Item</th><th>Description</th></tr>
<tr><td>284</td><td>19.6.1</td><td>The summary of "19.6.1 Control Status Register (CSR)" was corrected as indicated by the shading below:

The lower 8bits with the control status register (CSR) is prohibited from executing any bit manipulation instructions (Read-Modify-Write instructions).
Only in the case of HALT bits unchanged, use any bit manipulation instructions without problems (initialization of the macro instructions etc.).</td></tr>
<tr><td>286</td><td></td><td>The description "[Bit 0] HALT: Bus operation stop bit " of "■ Control Status Register (CSR)" was corrected as indicated by the shading below:

This bit controls the bus halt. The halt state of the bus can be checked by reading this bit.
Writing to this bit
0: Cancels bus operation stop
1: Sets bus operation stop
Reading this bit
0: Bus operation not in stop state
1: Bus operation in stop state

Note :
When write 0 to this bit during the node status is Bus Off, ensure that 1 is written to this bit.
Example program:
switch (IO_CANCT0.CSR.bit.NS)
{
case 0 : /* error active */
break;
case 1 : /* warning */
break;
case 2 : /* error passive */
break;
default : /* bus off */
for (i =0; (i <= 500) || (IO_CANCT0.CSR.bit.HALT == 0); i++);
IO_CANCT0.CSR.word = 0x0084; /* HALT = 0 */
break;
}
*: The variable " i " is used for fail-safe.</td></tr>
<tr><td>287</td><td>19.6.2</td><td>The following description was added to "Note" of "■ Conditions for Canceling Bus Operation Stop (HALT = 0)" as indicated by the shading below:

Note

- Canceling the bus operation stop after hardware reset or by writing 1 to HALT as above conditions is performed after 0 is written to HALT and continuous 11-bit High levels (recessive bits) have been input to the receive input pin (RX) (HALT = 0).
- Canceling the bus operation stop when the node status is changed to bus off as above conditions is performed after 0 is written to HALT and continuous 11-bit High levels (recessive bits) have been input 128 times to the receive input pin (RX) (HALT = 0). Then, the values of both transmit and receive error counters reach 0 and the node status is changed to error active.
- When write 0 to HALT during the node status is Bus Off, ensure that 1 is written to this bit.</td></tr>
</table>

Page	Item	Description
390	24.7 4	The shading below indicates changes made to Figure 24.7-2.