

## Errata

F<sup>2</sup>MC-16LX  
16-BIT MICROCONTROLLER  
MB90340 Series  
HARDWARE MANUAL

2004.11.16

Page	Item	Description																								
76	3.5.2	<p>Table 3.5-1 was corrected as indicated by shading below.</p> <ul style="list-style-type: none"> <li>• Error <table border="1"> <thead> <tr> <th>Address indicated by the stack pointer</th> <th>Cycle count compensation value</th> </tr> </thead> <tbody> <tr> <td>Internal area, even numbered address</td> <td>0</td> </tr> <tr> <td>Internal area, odd numbered address</td> <td>+2</td> </tr> </tbody> </table> </li> <li>• Correct <table border="1"> <thead> <tr> <th>Address pointed to by the stack pointer</th> <th>Interpolation value [cycles]</th> </tr> </thead> <tbody> <tr> <td>External 8-bit</td> <td>+4</td> </tr> <tr> <td>External even-numbered address</td> <td>+1</td> </tr> <tr> <td>External odd-numbered address</td> <td>+4</td> </tr> <tr> <td>Internal even-numbered address</td> <td>0</td> </tr> <tr> <td>Internal odd-numbered address</td> <td>+2</td> </tr> </tbody> </table> </li> </ul>	Address indicated by the stack pointer	Cycle count compensation value	Internal area, even numbered address	0	Internal area, odd numbered address	+2	Address pointed to by the stack pointer	Interpolation value [cycles]	External 8-bit	+4	External even-numbered address	+1	External odd-numbered address	+4	Internal even-numbered address	0	Internal odd-numbered address	+2						
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86	3.8	<p>The following sentence of “● When a stop request is issued from a resource” was added as indicated by shading below.</p> <ul style="list-style-type: none"> <li>• Error (36+6×Table 3.8-3 “Interrupt handling times”) machine cycles</li> <li>• Correct (36+6×Table 3.8-3 “Compensation values for interrupt handling times”) machine cycles</li> </ul> <p>The following sentence of “● When the counting is completed” was added as indicated by shading below.</p> <ul style="list-style-type: none"> <li>• Error (Table 3.8-1 “Execution time when the extended EI2OS continues” + Table 3.8-2 “Data transfer compensation values for extended EI2OS execution time” +21+6×Table 3.8-3 “Interrupt handling times”) machine cycles</li> <li>• Correct (Table 3.8-1 “Execution time when the extended EI2OS continues” + Table 3.8-2 “Data transfer compensation values for extended EI2OS execution time” +21+6×Table 3.8-3 “Compensation values for interrupt handling times”) machine cycles</li> </ul>																								
87		<p>Table 3.8-3 was corrected as indicated by shading below.</p> <ul style="list-style-type: none"> <li>• Error Table 3.8-3 Interrupt handling times <table border="1"> <thead> <tr> <th>Address pointed to by the stack pointer</th> <th>Interpolation value [cycles]</th> </tr> </thead> <tbody> <tr> <td>External 8-bit</td> <td>+4</td> </tr> <tr> <td>External even-numbered address</td> <td>+1</td> </tr> <tr> <td>External odd-numbered address</td> <td>+4</td> </tr> <tr> <td>Internal even-numbered address</td> <td>0</td> </tr> <tr> <td>Internal odd-numbered address</td> <td>+2</td> </tr> </tbody> </table> </li> <li>• Correct Table 3.8-3 Compensation values for interrupt handling times <table border="1"> <thead> <tr> <th>Address pointed to by the stack pointer</th> <th>Interpolation value [cycles]</th> </tr> </thead> <tbody> <tr> <td>External 8-bit</td> <td>+4</td> </tr> <tr> <td>External even-numbered address</td> <td>+1</td> </tr> <tr> <td>External odd-numbered address</td> <td>+4</td> </tr> <tr> <td>Internal even-numbered address</td> <td>0</td> </tr> <tr> <td>Internal odd-numbered address</td> <td>+2</td> </tr> </tbody> </table> </li> </ul>	Address pointed to by the stack pointer	Interpolation value [cycles]	External 8-bit	+4	External even-numbered address	+1	External odd-numbered address	+4	Internal even-numbered address	0	Internal odd-numbered address	+2	Address pointed to by the stack pointer	Interpolation value [cycles]	External 8-bit	+4	External even-numbered address	+1	External odd-numbered address	+4	Internal even-numbered address	0	Internal odd-numbered address	+2
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225	12.1	<p>The following description of " [bits 7 to 3] PONR, WRST, ERST, and SRST" in "■ Watch-dog timer control register (WDTC)" was added as indicated by shading below.</p> <p>[bit 7, bits 5 to 3] PONR, WRST, ERST, and SRST            These flags indicate the reset causes. The flags are set upon a reset as described in Table 12.1-1 "Reset cause registers".            All bits are cleared to "0" after the WDTC register is read. These bits are read-only bits.</p>																																																																										
243	13.4.2	<p>Figure 13.4-3 was corrected as indicated by shading below.</p> <table border="0"> <tr> <td style="vertical-align: top;"> <p>• Error</p> <p>bit 0</p> <table border="1"> <tr><td>CSTn</td><td>Comparison with timer for unit n (odd)</td></tr> <tr><td>0</td><td>Compare operation disabled for unit n</td></tr> <tr><td>1</td><td>Compare operation enabled for unit n</td></tr> </table> <p>bit 1</p> <table border="1"> <tr><td>CSTm</td><td>Comparison with timer for unit m (even)</td></tr> <tr><td>0</td><td>Compare operation disabled for unit m</td></tr> <tr><td>1</td><td>Compare operation enabled for unit m</td></tr> </table> <p>bit 4</p> <table border="1"> <tr><td>ICEn</td><td>Compare interrupt enable for unit n (odd)</td></tr> <tr><td>0</td><td>Output compare interrupt disabled for unit n</td></tr> <tr><td>1</td><td>Output compare interrupt enabled for unit n</td></tr> </table> <p>bit 5</p> <table border="1"> <tr><td>ICEm</td><td>Compare interrupt enable for unit m (even)</td></tr> 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