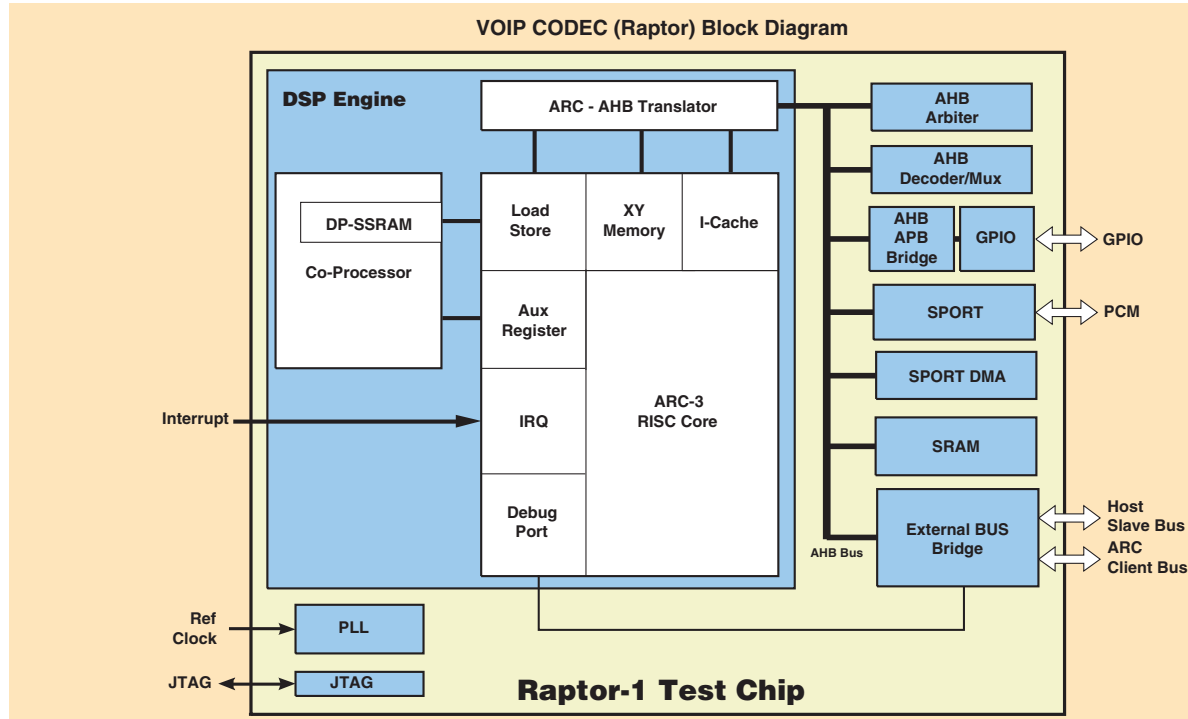


VOIP CODEC



Features

- Four simultaneous and independent voice channels each supports
 - G.168 Echo Cancellation
 - Vocoder: G.711, G.726, G.728, G.729AB, G.729e
 - DTMF encode and DTMF decode
 - Dial tone generation
 - Reverse ring-back generation
- Bus master interface with built in DMA for accessing host and system memory. Shared system memory eliminates need for dedicated memory
- PCM Audio CODEC interface (SPORT) with AC'97 compliant audio CODEC
- Extended ARC-3 DSP core with Co-Processor provides efficient & flexible soft solution for algorithm updates and optimization
- Complete evaluation system
- Boundary scan test (JTAG)
- 3.3V I/O, 2.5 V Core, 0.25µm technology (Test chip)
- 304 PQFP (Test chip)

Applications

- Residential Gateway
- IP Phone
- Cable Modem
- Computer Telephony
- Wireless LANs
- Fixed Wireless
- Mobile Ad Hoc Networks
- Access Points

VOIP CODEC

► Overview

VoIP Codec is designed for implementing speech Vocoders to support VOIP applications for Customer Premises Equipment (CPE). Up to 4 channels of audio can be supported simultaneously. The current implemented Vocoders are G.711, G.726, G.728, G.729AB, and G.729E. Any combination of Vocoders is supported and each channel provides echo cancellation (G.168), DTMF generation/detection, and jitter buffering. The DSP engine is based on ARC-3 Processor utilizing its DSP extensions together with extensive hardware accelerators

► DSP Engine Architecture

DSP engine provides the means for in-line and parallel acceleration of algorithms. In-line acceleration is accomplished through the addition of select instructions to the ARC execution unit while parallel acceleration is accomplished through a Co-Processor unit. The ARC core is interfaced to the memory and peripheral subsystems through several translators in which the subsystems are connected to a single or multiple AHB compliant buses. The ARC core has three separate memory clients (instruction cache controller, load/store unit, and X-Y memory burst controller), each with its own separate bus that requires access to the internal AHB bus. Each memory client in turn has its own dedicated ARC-AHB translator logic block, which provides access for that memory client to the AHB bus as a bus-master. DSP engine consists of a baseline ARC 3.0 core with several additional features and extensions to support specific instructions. This is summarized in the following.

Instruction Set Architecture:

- Register file
- Fast load returns
- Fast 32x32 barrel shifter
- Swap
- Min/Max
- Normalize

(Co-Processor). This provides a flexible and powerful soft solution for future algorithm enhancements and upgrades. Test chip is offered as a Soft Core Silicon for ASIC & SOC designs. A top-level block diagram of the chip is shown above.

A complete system designed around Raptor Test Chip is also available for evaluation purposes only to provide a home gateway solution. This system uses an ARC-3 processor as its host to run application software with a Real Time Operating System, Network Stack and MGCP protocols.

DSP Configuration:

- Dual 16x16 XMAC
- Saturated add/subtract
- XY memory. The X-Y memory and associated controller supports 16 and 32-bit data addressing modes, and post and pre-address update modes with variable offsets.

Cache Configuration:

- Direct mapped I-cache and cache controller with coderam supports algorithms handled on chip
- Local Load Store RAM. The Load Store RAM is a fast access single cycle data RAM which overlays a section of the main memory, so the data access need not go through the Memory Arbitration Unit and the Memory Sequencer to the external memory. It is like a local data cache and typically can be used as a stack accelerator.

Hardware Accelerator:

- ARC Co-Processor interface and the Co-Processor module
The Co-Processor consists of a FIFO, a Dual port Synchronous SRAM, and the data path logic. The FIFO is used only for parameter passing to the data path state machines. The SRAM is connected to the local load/store bus from the ARC's Load Store Unit (LSU). The Co-Processor control and status signaling communicates through ARC auxiliary register space. The Co-Processor Unit consists of four MACs.

Debug of the ARC processor is done through the ARC Debug Interface Module, which is accessible from the host bus via a secondary port off of the Host Interface.

► Evaluation System

The Evaluation System provides a complete Residential Gateway Solution. A hardware block diagram of the Evaluation System is given in Figure 1. This board can support four channels voice interface. The interface to the network is through a 10BaseT Ethernet. Software configuration of the system is summarized in Figure 2.

The MGCP protocol is by Radvision. The RTOS and Network Stack are by Accelerated Technology (Nucleus).

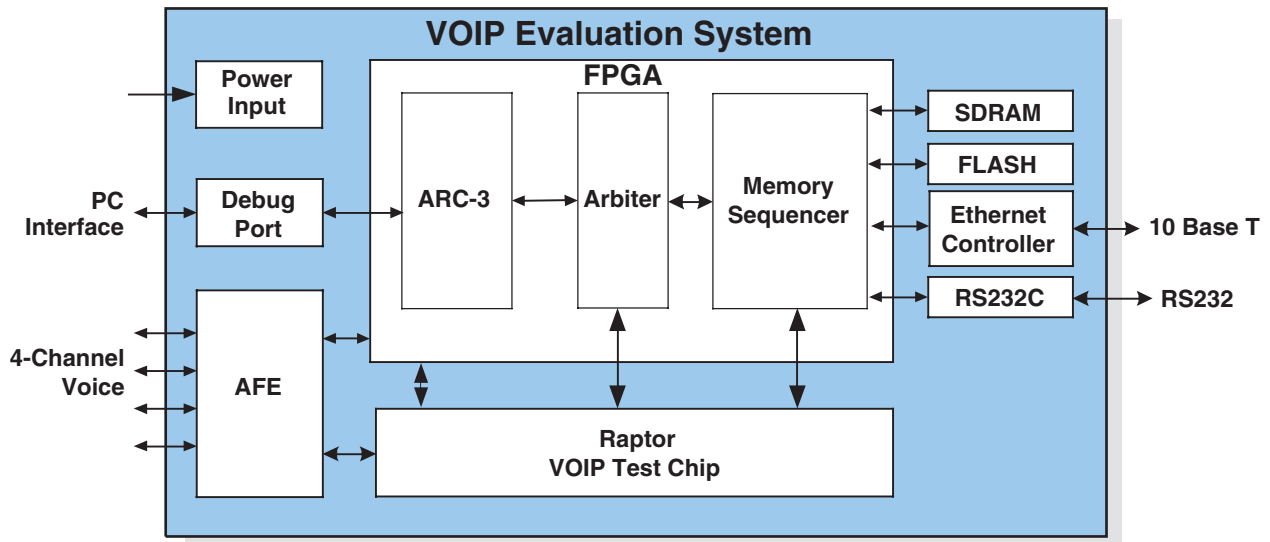


Figure 1. Hardware Configuration

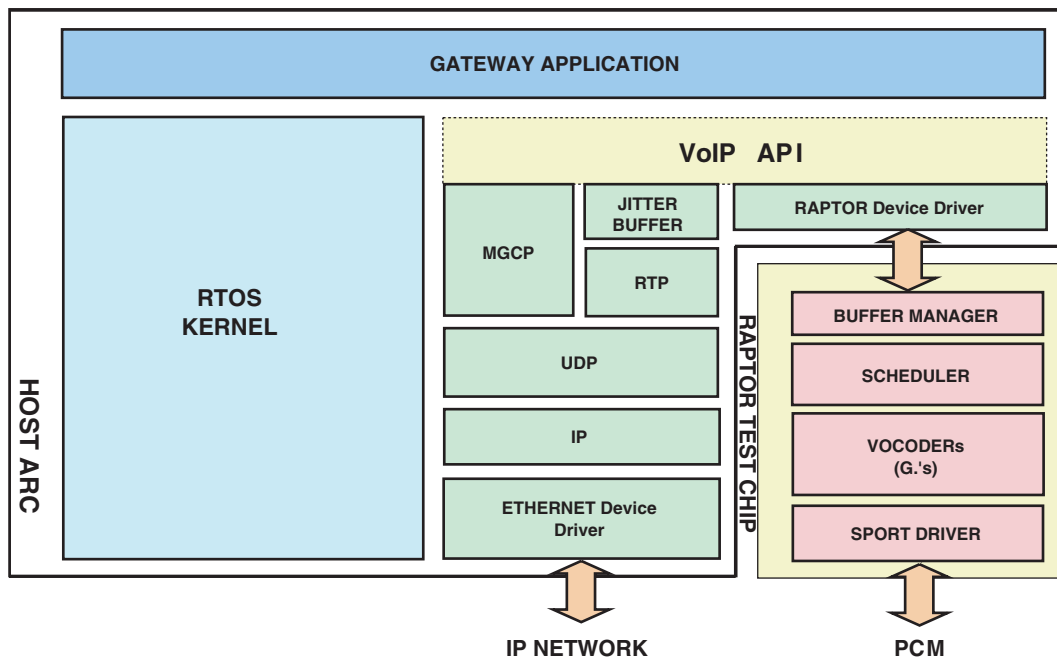
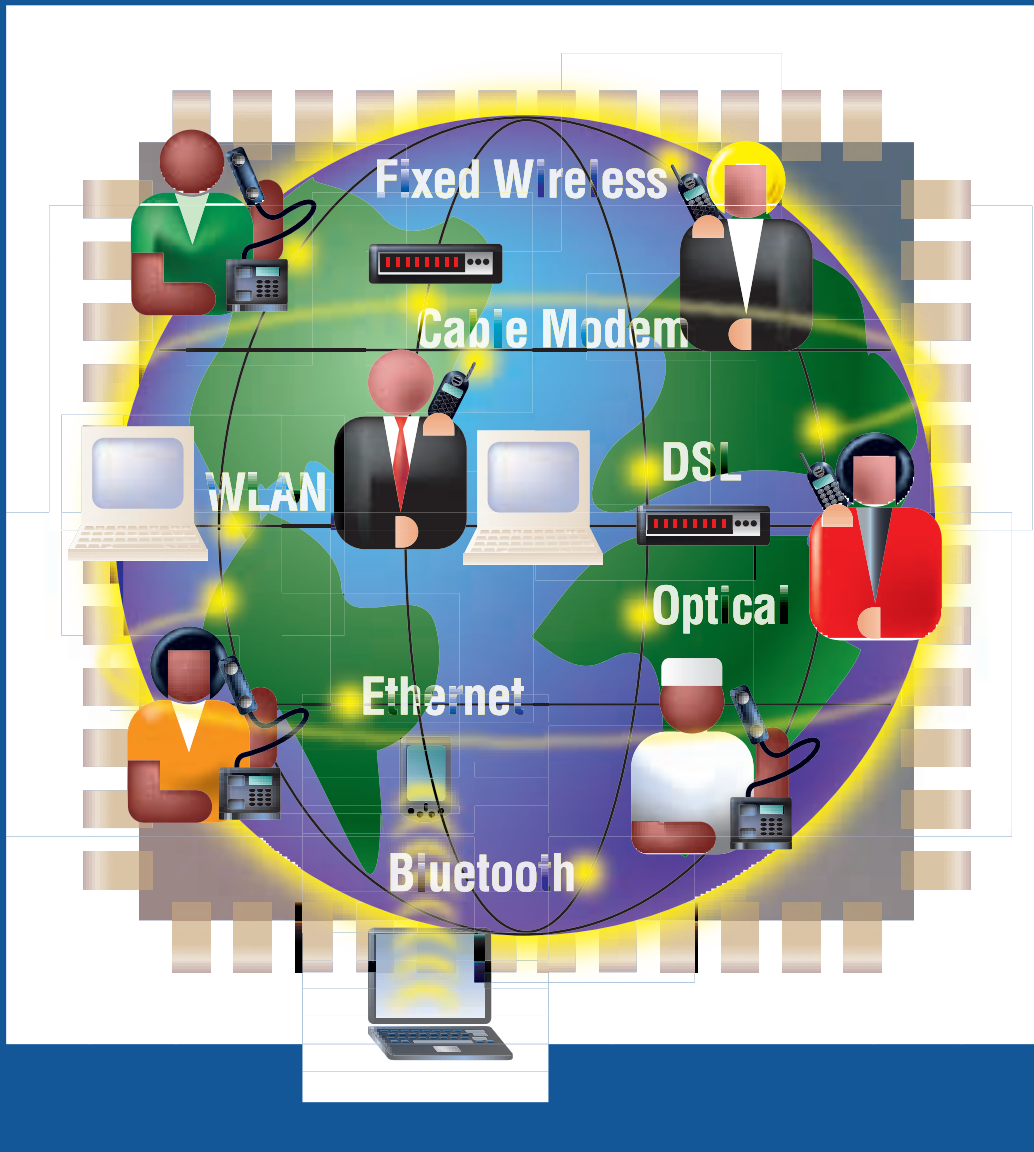


Figure 2. Software Configuration

VoIP

Different Cultures, One Voice



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