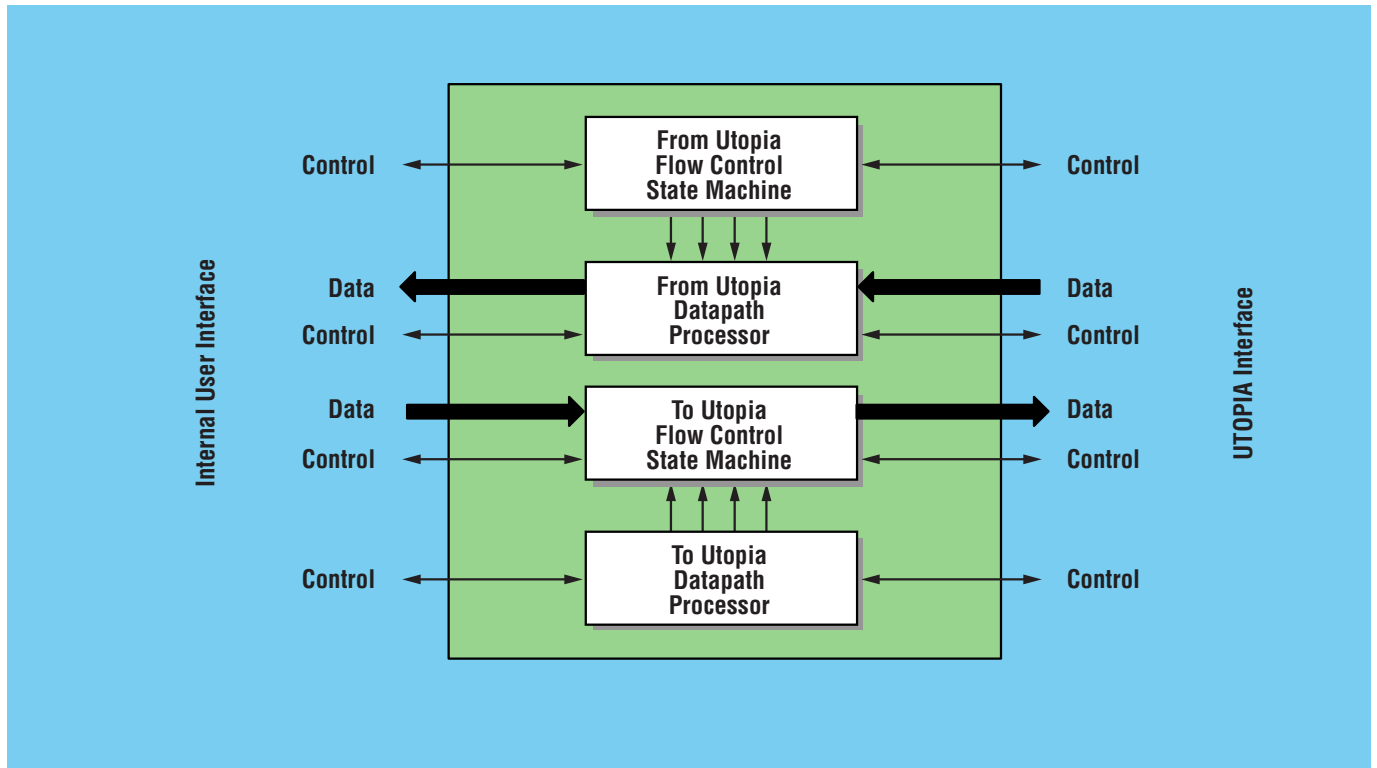


Utopia Level II / I Interface Core



► Features

- PHY layer or ATM layer operation
- Level II and Level I support
- Cell and octet-level handshake support in Level I
- Supports 8- or 16-bit Utopia Interface; simple interface to cell buffer macro
- Basic polling interfaces allowing user defined polling schemes
- Supports a range of cell sizes from 52 to 64 bytes
- Support flexible, user-configurable polling schemes via simple synchronous interfaces
- Operates at 52 MHz

► Benefits

- Support for ATM Forum specification Level I and II
- Simple synchronous interface to cell buffer macro
- Allows target device address decoding or polling schemes to be attached externally

Utopia Level II / I Interface Core

Description

The Utopia Level II interface provides a standard interface between a single ATM layer device and multiple PHY layer devices. The macro can also be configured as a Utopia Level I interface, which is used to provide a standard interface between a single ATM layer device and a single PHY layer device. The macro may be used in either ATM Layer or PHY Layer mode. Eight or 16-bit Utopia data is supported. The macro also performs data flow control between the two layers: parity checking and port address/poll address routing.

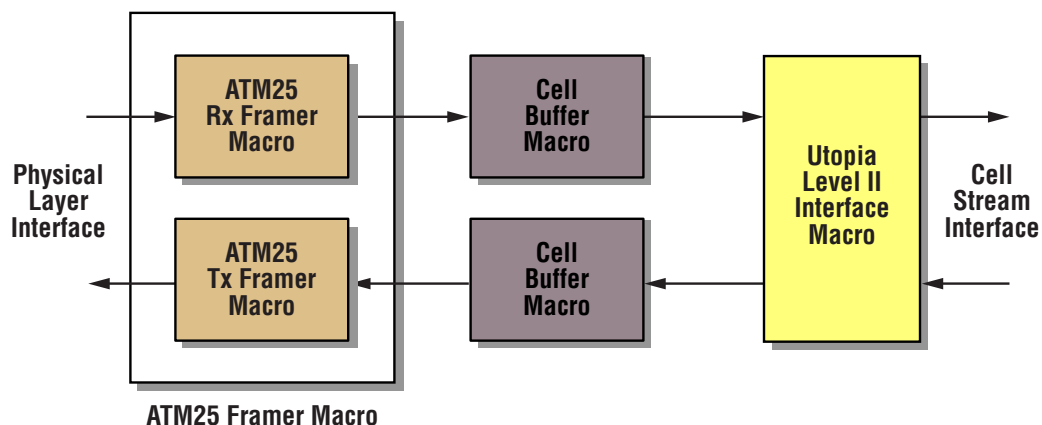
A routing tag (0–15 bytes long) may be added to each ATM cell, which is treated as an extension of the cell. Likewise, an ATM cell may include an HEC field. Corresponding UDF1 and UDF2 bytes are included in the cell, depending on whether 8- or 16-bit mode is selected.

This core is ideally suited for a variety of applications in the local area networking (LAN) space for LAN switches and ATM access switches. It can also be employed in wide area networking (WAN) space for WAN switches, routers, as well as applications in Central Office (CO) and Consumer Premise Equipment (CPE) equipment.

Deliverables

A Fujitsu application engineer works with the customer to help them select the process technology that best suits the customer's specific need. After the technology is selected, the following deliverables are supplied to the customer:

- Encrypted RTL source codes written in Verilog HDL, representing the entire hierarchical Utopia II/I core design
- Encrypted Verilog Test Bench for functional verification
- A hierarchical gate-level netlist of the framer core



In a typical application, the Utopia Level II Interface macro provides connectivity between the physical layer and the ATM layer in an ATM 25 Mbps Framer device.

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