

Application Note

How to replace SRAM with PSRAM (Mobile FCRAM)

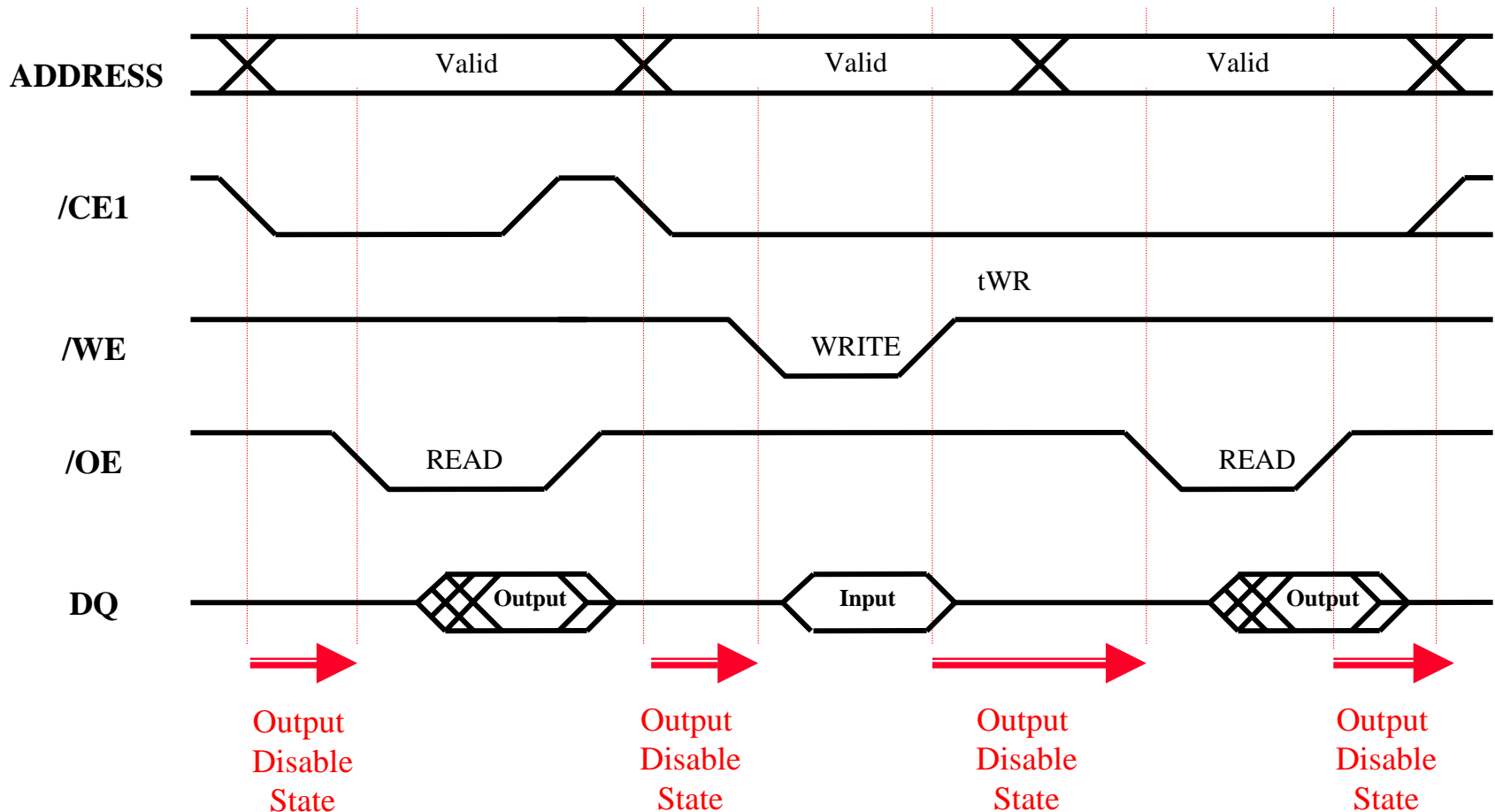
Fujitsu Microelectronics Limited

- Difference between SRAM vs PSRAM (Mobile FCRAM)
 1. Cell structure
 - 1-1. Logic condition restriction
 - 1-2. Electrolytic capacitor
 2. Peripheral circuit
 - 2-1. Input signal transition spec
 - 2-2. Timing spec
 3. Power Up sequence
 4. Signal Functionality
 - 4-1. CE2
 - 4-2. /LB & /UB
- Instruction for use

- SRAM uses 6 transistors cell
 - Stable latching circuitry by Flip Flop
- PSRAM uses DRAM cell consists of 1 capacitor and 1 transistor
 - Stored data discharge due to internal leak current
 - Require restore operation after read due to destructive read method
- Notice
 - Satisfy logic condition restriction (See P4)
 - PSRAM automatically control internal refresh and precharge operation
 - Logic condition must be managed to enable appropriate internal refresh and precharge control
 - Put electrolytic capacitors between VDD and VSS pins (See P5)
 - to sustain peak current related with internal refresh operation
 - Satisfy VDD min spec for data retention
 - Data retention voltage spec is same as operating voltage spec
 - Not support low voltage data retention function

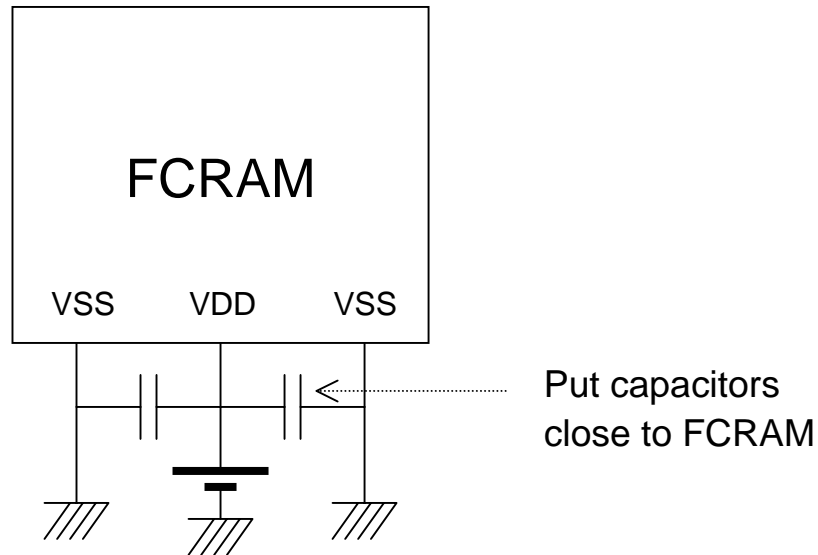
1-1. Logic condition restriction

- **Must not keep “Output Disable state” ($/\text{CE}1=\text{L}$, $/\text{OE}=\text{H}$) longer than 1us**
 - **Might issue specially for slow speed operation**



1-2. Electrolytic capacitor

- To sustain voltage variation due to large peak current related with internal refresh operation
 - Recommend to put electrolytic capacitors of 0.1uF to 0.2uF between VDD and VSS pins



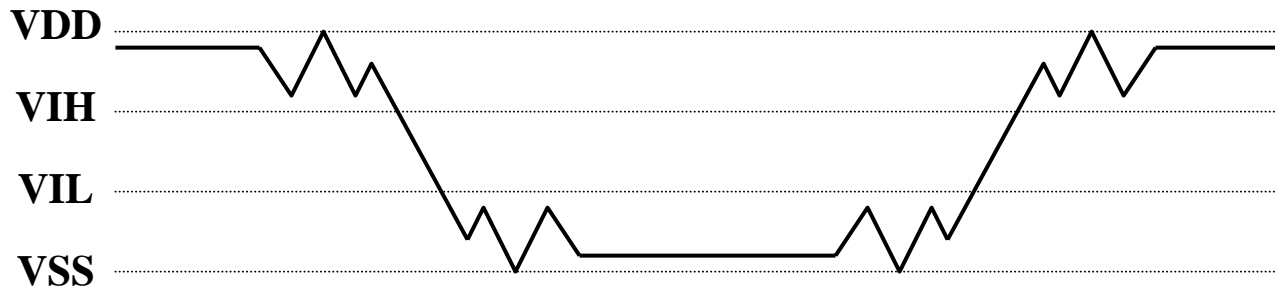
2. Peripheral circuit

- SRAM operation starts when control signal logic is valid
- PSRAM (FCRAM) operation starts when transition of control signal is detected
 - Unstable transition signal cause wrong operation (sensitive to glitch)
 - PSRAM operations can not be stopped/changed once the operation cycle starts due to internal refresh and restore operation
 - Related timing specs must be satisfied
- Notice
 - Input signal transition spec (See P7)
 - Setup / Hold timing spec (See P8-11)
 - PSRAM original spec related with internal refresh and precharge operation
 - Please refer to product datasheet for details of actual timing specs.

2-1. Input signal transition spec

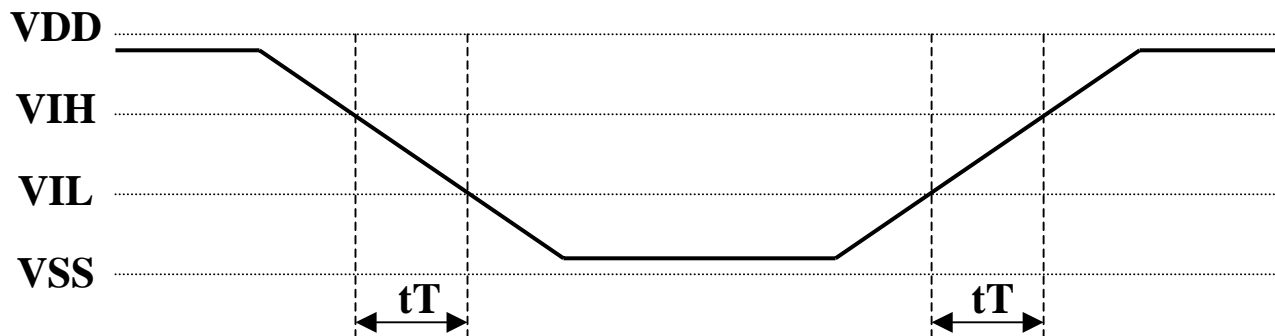
■ Glitch criteria

- Signal transition is defined between V_{IH} and V_{IL}
- Signal variation over V_{IH} and under V_{IL} is not included



■ Input signal transition spec

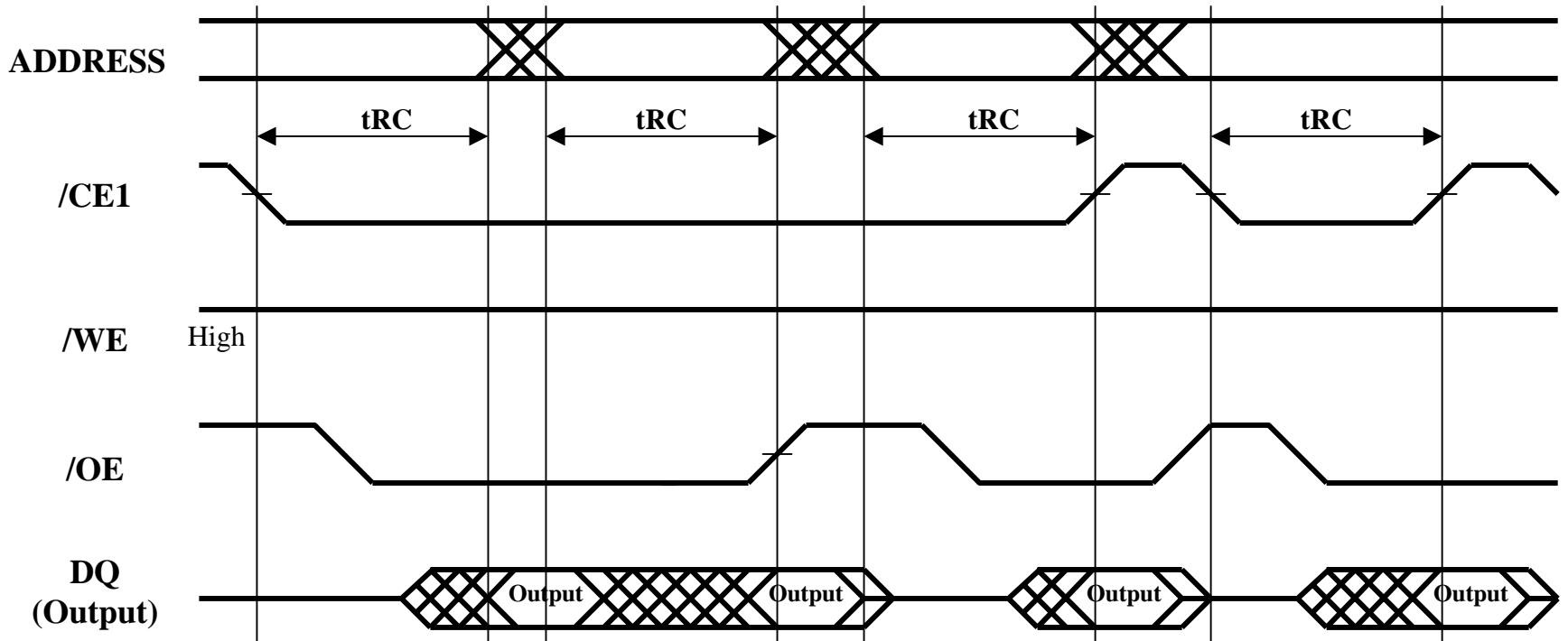
- Max transition time spec is 25ns



2-2. Timing spec (1)

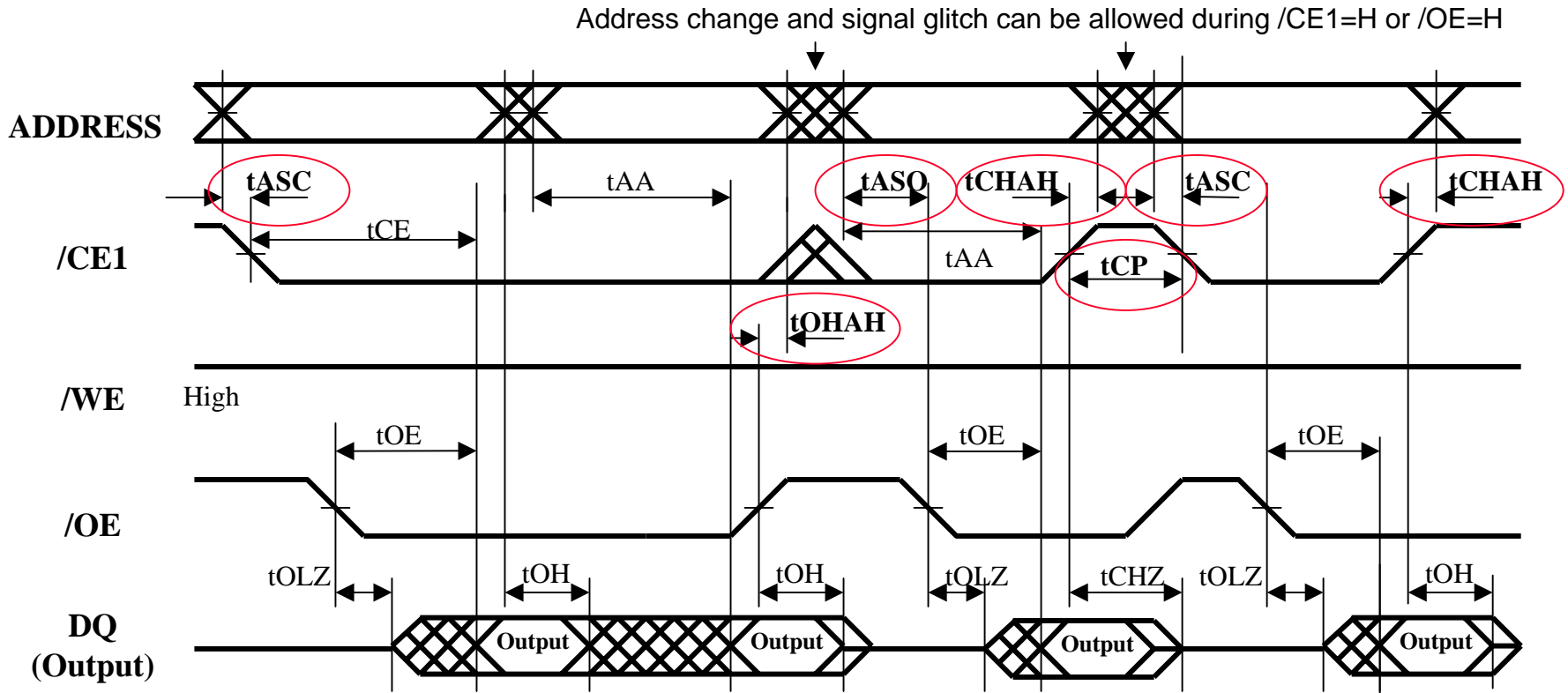
■ Cycle time spec during read operation

- The cycle time is specified from transition of /CE1 and addresses
 - Min and Max cycle time spec must be satisfied



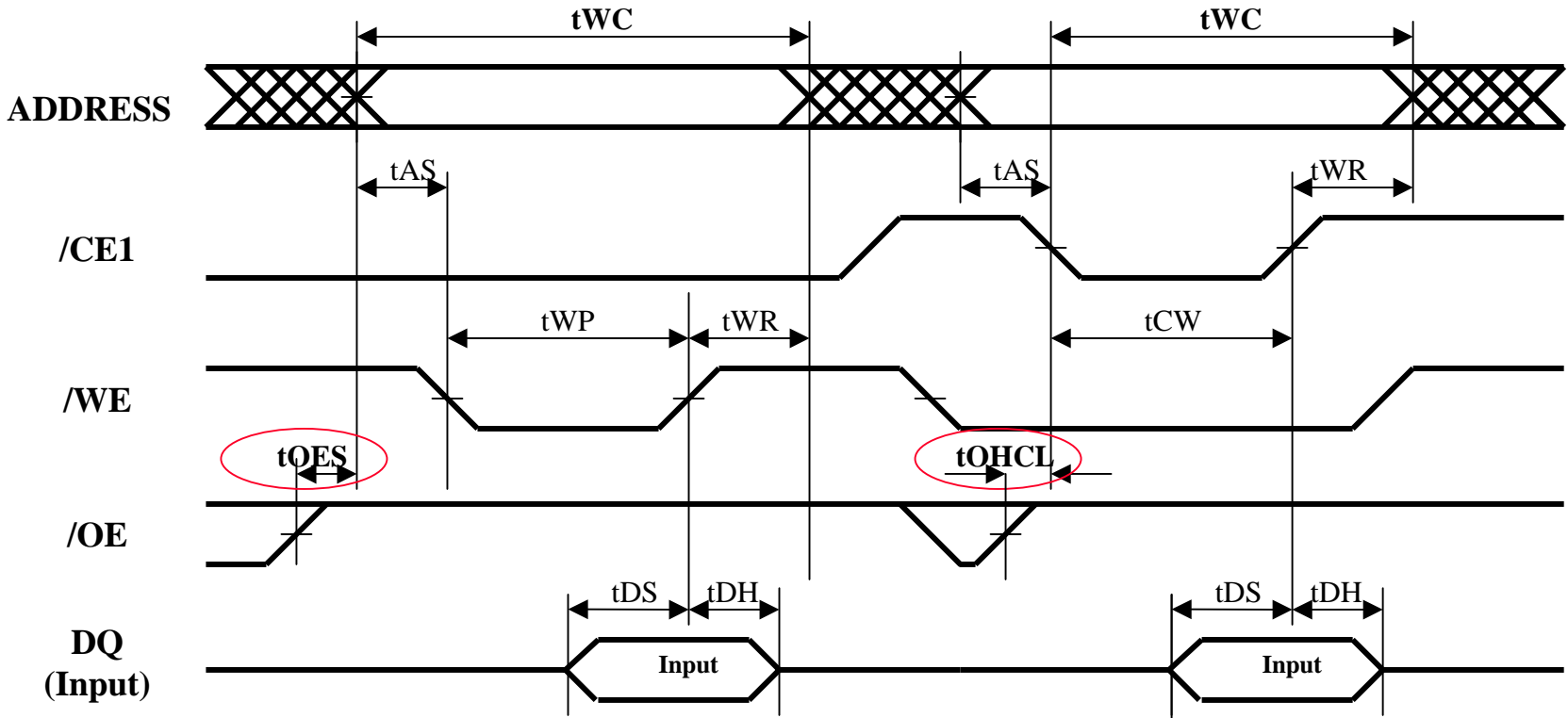
2-2. Timing spec (2)

■ Setup and Hold time during read operation



2-2. Timing spec (3)

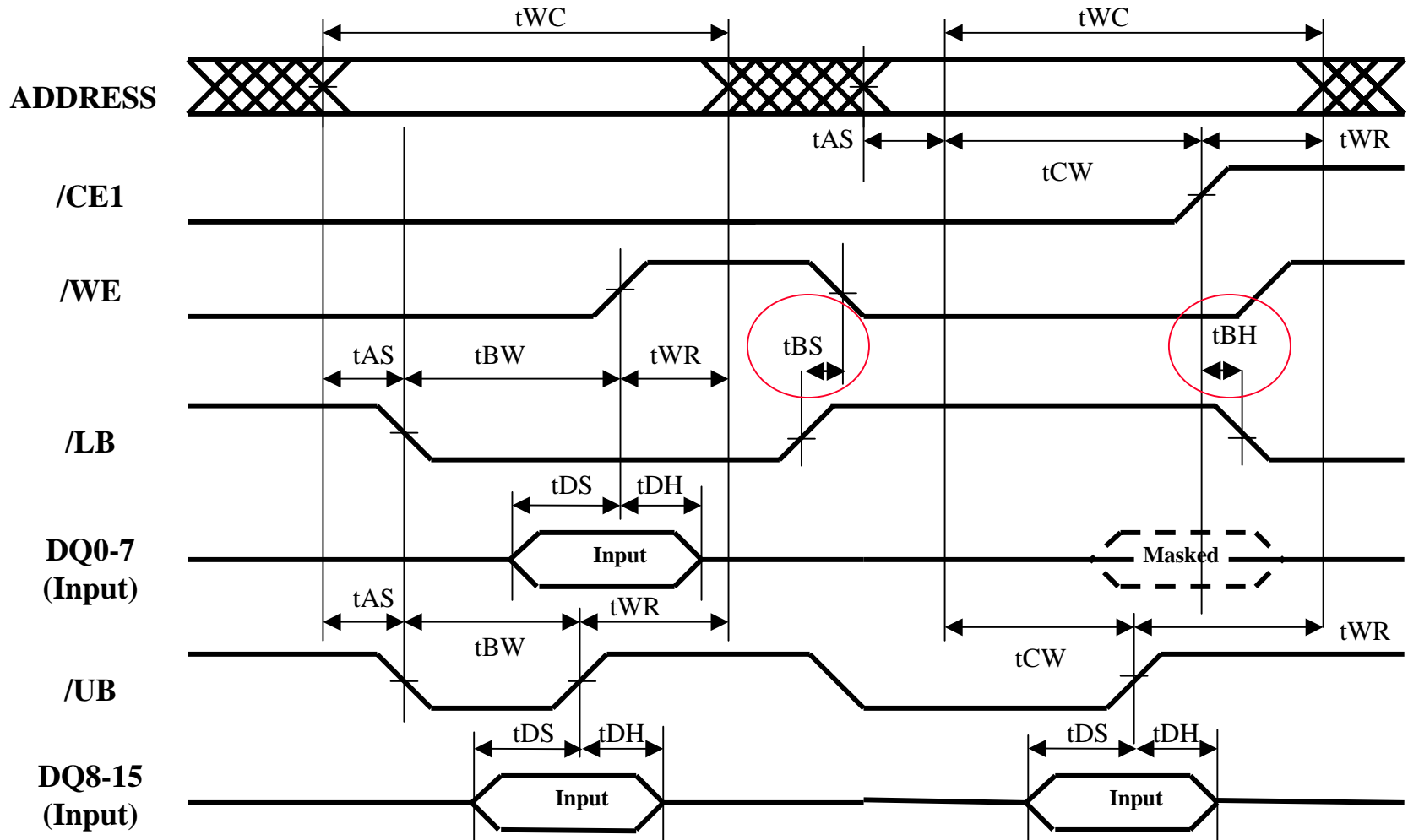
- /OE must be kept high during write operation



2-2. Timing spec (4)

Byte mask during write operation

- When byte mask function is used, specified setup / hold time of /LB&/UB must be satisfied



3. Power up sequence

- SRAM can operate when internal voltage is charged
- PSRAM (FCRAM) need initialize time to enable internal voltage regulator
 - PSRAM can operate after initialize time of $t_{CHH}=300\mu s$ when internal voltage become stable
 - See datasheet for power up related specs and timing example

4. Signal Functionality (1)

4-1. CE2

- SRAM can use CE2 for read and write operation control
- PSRAM (FCRAM) use CE2 for power down control
 - CE2 must be kept high during read and write operation

4-2. /LB, /UB

- SRAM use /LB, /UB signal which has same functionality as /WE
- In PSRAM (FCRAM) case, /LB, /UB setup and hold time for /WE (or /CE1) must be satisfied
 - /LB, /UB can be controlled synchronous with /WE (or /CE1)

4. Signal Functionality (2)

■ Function truth table

- Note that CE2, /LB and /UB signal functionality as shown in the following function truth table

Mode	/CE1	CE2	/LB	/UB	/WE	/OE	DQ0-7	DQ8-15
Power Down	X	L	X	X	X	X	Hi-Z	Hi-Z
Read	L	H	L	L	H	L	Output	Output
Read Lower Byte	L	H	L	H	H	L	Output	Hi-Z
Read Upper Byte	L	H	H	L	H	L	Hi-Z	Output
Write	L	H	L	L	L	H	Input	Input
Write Lower Byte	L	H	L	H	L	H	Input	X
Write Upper Byte	L	H	H	L	L	H	X	Input
Output Disable	L	H	X	X	H	H	Hi-Z	Hi-Z
Standby	H	H	X	X	X	X	Hi-Z	Hi-Z

1. Logical Design

- Check Control signal compatibility for CE2, /LB, /LB signal (See P14)

2. Timing Design

- Must satisfy PSRAM original timing spec (See P4, P8-11)
 - Logic condition restriction
 - Specific timing spec related with internal refresh and precharge
- Must satisfy input signal transition time spec (See P7)

3. Supply voltage design

- Insert appropriate capacitors (See P5)
- Must satisfy PSRAM power up sequence