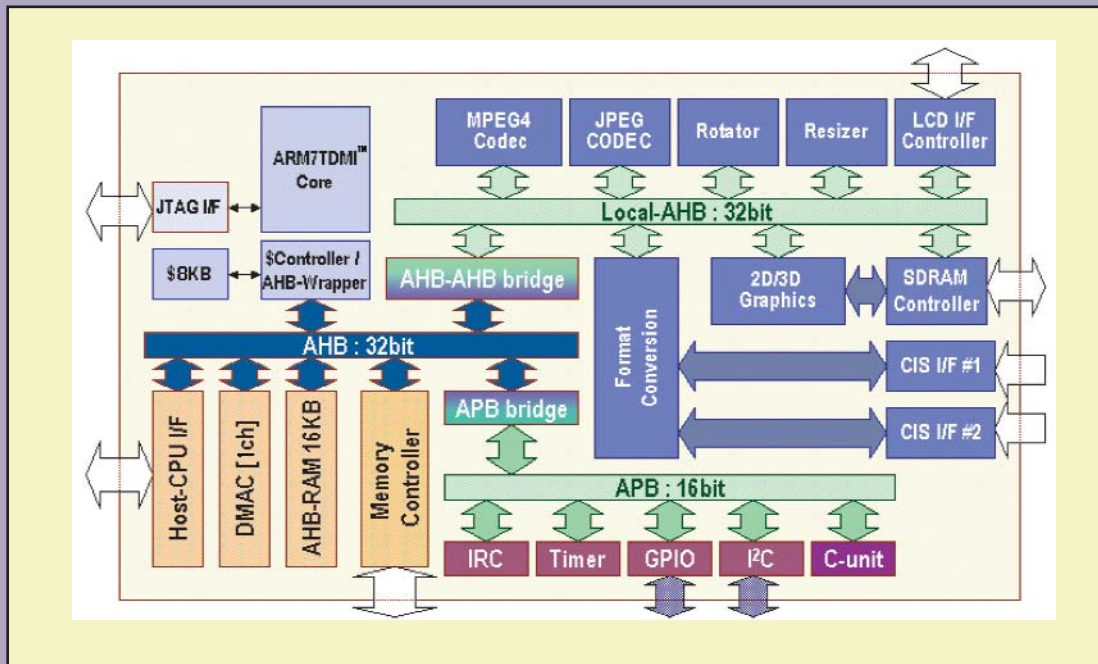


Mobile Media Processors



► Description

Fujitsu MMP products, MB86V00 and MB86V01, are designed to function as visual subsystems for cellular phone and other mobile applications. Key functions such as JPEG and MEG-4 codecs are supported in hardware. Moreover, these particular implementations have been highly optimized for operation in a small screen environment (VGA or below). Special algorithms and clock gating techniques serve to provide excellent image quality while keeping power consumption at a minimum - as low as 13 mW (operational). The devices feature multiple camera interfaces for new generation cell phones that offer both an outward viewing camera (for taking scenic or portrait pictures) and a self-portrait or videophone camera. The maximum resolution for the camera interfaces are VGA (Interface #1 or videophone camera) and 2.4 Megapixel (Interface #2) for the full-featured camera. The Fujitsu MMP enables images to be resized, rotated, and viewed on two LCD screens simultaneously.

Games and other graphic-based programs are also supported using the high-powered 2D/3D graphics engine included in all Fujitsu MMP products. Fujitsu has many years of experience in developing special purpose graphics controllers for use in automotive in-dash navigation and entertainment systems. Many of the special functions and features required in these automotive applications are also required in 3G cell phones and the latest generation PDAs. For example, Fujitsu MMPs provide hardware support for producing multiple display windows that can be individual resized and alpha blended. In addition, the graphics core offers special line drawing functions, BitBlt, texture mapping and other high-end graphics operations.

The MMPs are housed in compact fine pitch BGA (.5mm pitch) that measure 10mm by 10mm. The MB86V01 features a system-in-package (SIP) design that includes 64Mbit of SDRAM for storing captured or downloaded images.

Mobile Media Processors

► Specifications

MPEG4 codec

- Version 1 Simple Profile, upto Level 3
- Full hardware implementation for minimum power consumption
- CIF 15fps (full duplex)
- VGA 30fps (half duplex)
- Supports Motion Estimation (ISO/IEC 14496-7) and RVLC

JPEG codec

- Can support upto 2048 x 2048 image size
- Huffman and quantization tables for JPEG processing
- Supports 422, 411 and 420 sampling formats

Peripherals

- GPIOs
- I2C interface
- UART interface
- PWM

2D/3D GDC

- Alpha Blending
- Texture Mapping
- Z-Buffer
- Polygon Drawing
- 8, 16 and 24 bpp color depths
- Bit BLT
- Performance upto 500K polygon/sec and 75M pixel/sec

Camera Interface

For both camera interfaces

- | | | |
|-----|------|------|
| Max | 1616 | 1236 |
| Min | 24 | 24 |
- Supports YUV 422, 8-bit parallel interface
 - Input clock upto 48 MHz
 - Image down scaling to arbitrary size
 - Cubic and Bilinear filter to minimize image deterioration during size scaling

Host CPU Interface

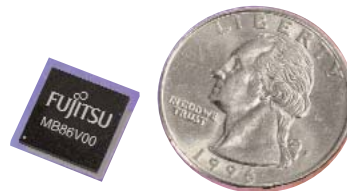
- 8/16-bit parallel interface
- Narrow and Wide address modes
- Register control
- Display list transfer
- MPEG4 codec data read/write
- Read/Write to SRAM area
- Direct read/write from LCD

ARM7TDMI™

- Implemented for internal module control, AE/AF/AWB processing and Host CPU communication
- Main bus conforms to AHB/APB (AMBA) standard
- Cache controller and memory (8kB)
- Internal SRAM (16kB)
- External memory (SRAM/Flash) controller
- Timers

► Features

- MMP available in either SIP (with 64Mbit VRAM) or single chip (no memory)
- Full hardware implementation of multimedia functions, which dramatically reduces power consumption and improves system performance
- Cubic and Bilinear filters to minimize deterioration during size scaling of the camera image
- Separate bus interfaces for CMOS camera module, LCD and Host CPU (baseband) - significantly reduces internal data traffic to give a superior multimedia performance
- Motion estimation (ISO/IEC 14496-7 compliant) and RVLC functions of the MPEG4 codec to suppress the image quality degradation



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