

8-bit Microcontroller Featuring Fast Processing, Low Voltage, and Low Power Consumption Operation

F²MC-8FX Family

This product family features the maximum operation frequency of approximately 3 times that of the conventional F²MC-8L Family and 5 times the maximum processing capability due to the optimized CPU core. In addition, by adopting 0.35 μ m low leak process technology, mask ROM models can operate on 1.8 V in the 1 μ A low power consumption operation mode.

Product Description

Because the latest digital home electronics appliances and mobile system products have been coming out with advanced features, the 8-bit microcontrollers need to provide fast processing and reduced power consumption. In order to meet these demands, FUJITSU has developed the F²MC-8FX Family.

Photo 1 MB95FV100 External View

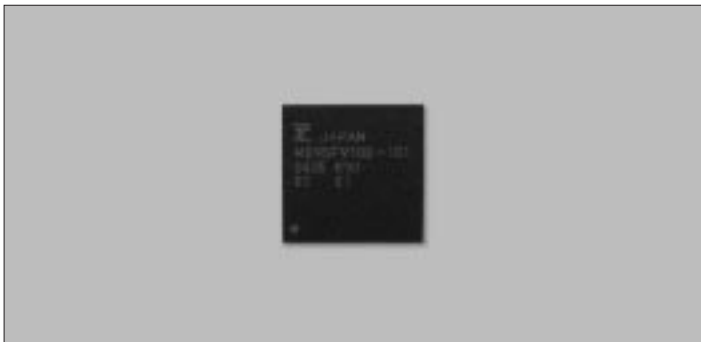


Fig.1 illustrates the product concept of the F²MC-8FX Family.

This product family features a maximum operation frequency of 10 MHz, approximately 3 times that of the conventional F²MC-8L Family, and 5 times the maximum processing capability owing to the optimized CPU core. In addition, by adopting 0.35 μ m low leak process technology, mask ROM models can operate on 1.8 V in the 1 μ A low power consumption

Photo 2 MB2146-09 External View



operation mode (clock mode^{*1}). This product family is designed to ensure compatibility with the conventional F²MC-8L Family for all instructions except that relating to division. As such, it allows easy migration from the F²MC-8L Family.

Fig.2 shows the positioning of this product family in FUJITSU microcontroller families.

For the development environment, this product can offer MB2146-09, a 55g lightweight and compact hardware development tool by incorporating BDSU^{*2} in an evaluation chip MB95FV100.

Fig.3 presents the product lineup plan for this product family.

FUJITSU will develop packaged products in this family ranging from 20-pin to 100-pin designs. By the end of 2004, FUJITSU will offer MB95FV100, an evaluation product that is commonly applicable to this family, the 64-pin MB95100/H Series, and the 48-pin MB95110 Series. This product family is designed based on standardized specifications. As such, a single chip of MB95FV100 allows the development of 20-pin to 100-pin designs.

Product Features

Fast processing

- Maximum operating frequency: 10 MHz

The instruction cycle is reduced, on average, to two-thirds

through optimization of the CPU bus architecture of the conventional F²MC-8L Family.

- The maximum processing capability is approximately fivefold that of the F²MC-8L Family.

Low voltage operation

- 3 V models can operate on a minimum voltage of 1.8 V.
- 5 V models can operate on a minimum voltage of 2.2 V (Target Spec).

Low power consumption operation

- Power-saving operation is available due to the adoption of 0.35 μm low leak process technology.
- A 1 μA low current consumption operation can be achieved in the clock mode (operation on 3 V).

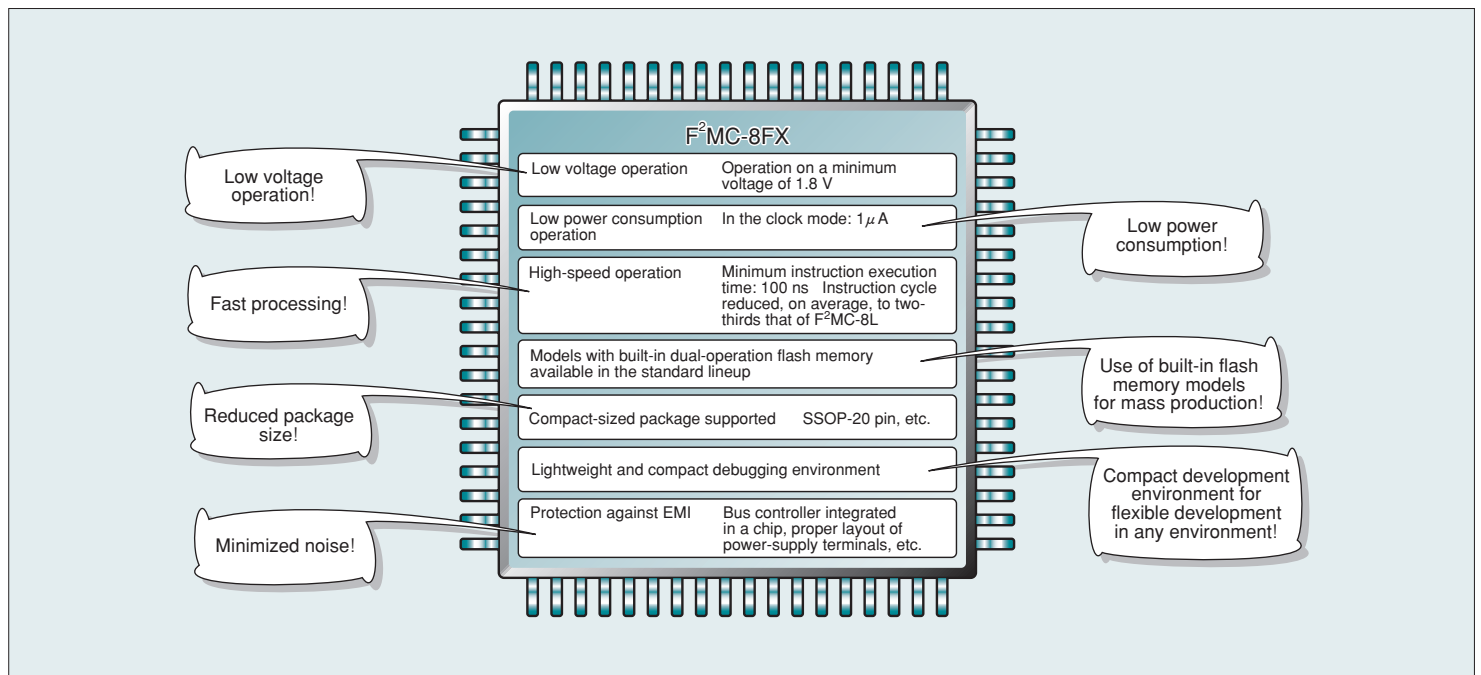
Dual-operation flash-memory-integrated models are available in the standard lineup

While a program is being run in one bank, rewriting can be completed in the other. A reduction in board surface area can be achieved by minimizing the number of external memory component parts.

Enhanced arithmetic operation function

The division instruction is enhanced to 16-bit÷16-bit. All other instructions are compatible with those for F²MC-8L.

Figure 1 F²MC-8FX Family Product Concept



- F²MC-8FX: T (16-bit) ÷ A (16-bit) = A (Quotient: 16-bit)
 ...T (Remainder: 16-bit)
- F²MC-8L: T (16-bit) ÷ AL (8-bit) = AL (Quotient: 8-bit)
 ...TL (Remainder: 8-bit)

Reduced instruction cycle

The internal bus of the pipeline structure and the adoption of the pre-fetch buffer have achieved a reduced instruction cycle primarily involving the operation command. **Table 1** presents examples of the reduced instruction cycle.

Clock multiplier circuit

- The CPU provides a maximum operating frequency of approximately 3 times that of conventional CPUs.
- Adoption of the multiplier circuit allows high-speed operation utilizing an inexpensive low-speed radiator.

Table 2 shows clock frequency and gear ratio.

Expanded interrupt level

The user-definable interrupt level is expanded to four levels instead of the conventional three levels.

Expanded direct-access area

The lower 3 bits of the register bank point (RP) allow remapping

of the direct area (equivalent to 128 bytes) accessible with bit/byte.

Fig.4 shows conversion of direct-access domain.

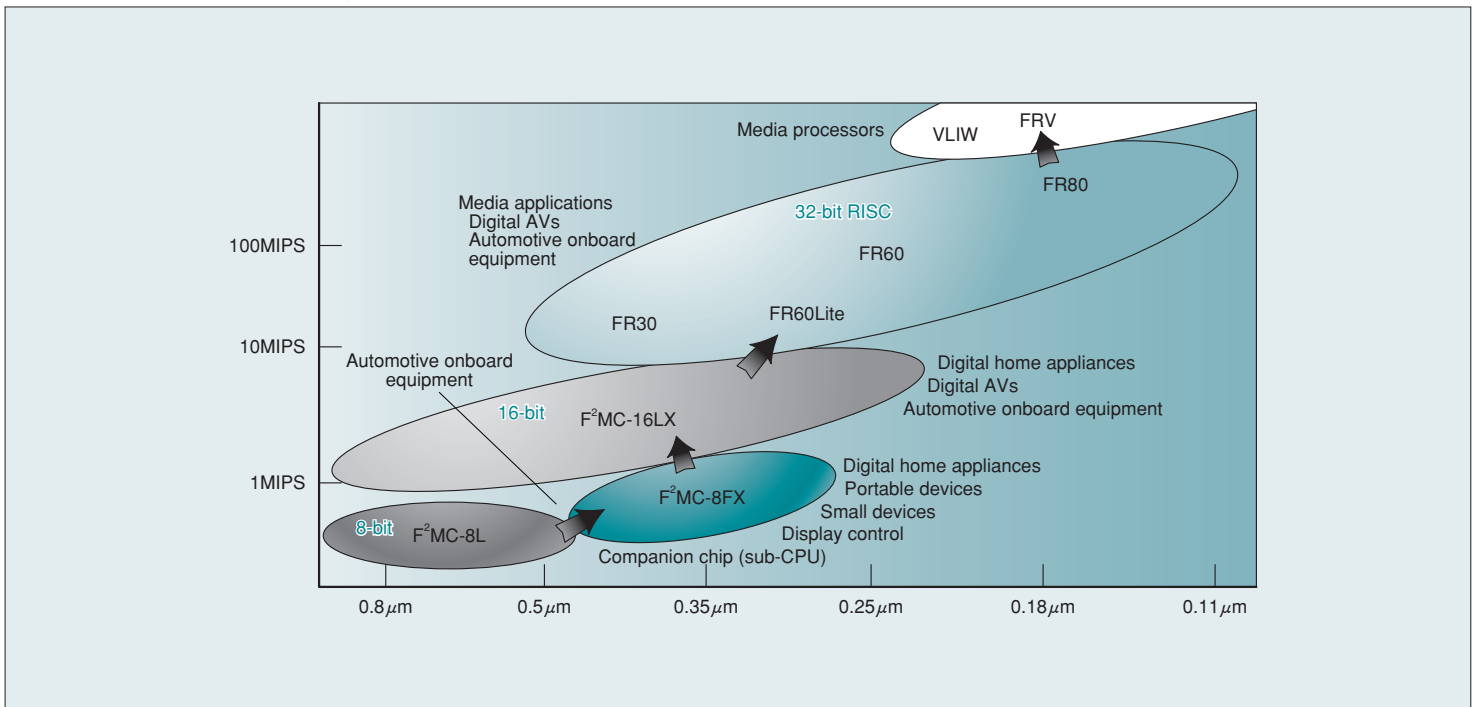
Table 3 lists the product configuration of this family and a description of the available functions. **Fig.5** presents a block diagram of the MB95100/H Series, and **Fig.6** presents a block diagram of the MB95110 Series.

Development Environment

Fig.7 presents the configuration of the development environment hardware for this product family, and **Table 4** provides a list of the development tools supported.

For the hardware configuration, a PC and an MB95FV100-installed adaptor board (W40mm×D40mm×H14.6mm) are connected through the MB2146-09 (W40mm×D200mm×H25mm), an adaptor designed specifically for background monitor debugging. For installation of the adaptor board into a user system board that has a pattern printed for mass-production packages, a package conversion header board (W40mm×D200mm×H20.7mm) is used. The adaptor board can be directly installed to the evaluation board that incorporates a socket for it.

Figure 2 Positioning of F²MC-8FX Family



In addition, a through hole is provided to allow checking of all terminals with a total of 16 LEDs installed.

Software can be developed in a suitable environment supporting the F²MC-8FX-compatible version of FUJITSU's integrated development environment SOFTUNE™ V3.

Table 5 lists the debugging functions of the development environment for this product family. *

*2: BDSU (Background Monitor Debug Support Unit): A circuit that allows the debugging function to operate without the use of user-using functions (memory, I/O terminals, etc.)

* SOFTUNE is a trademark of FUJITSU LIMITED.

* Other product names and company names referenced in this article are the trademarks or registered trademarks of the respective companies.

NOTES

*1: Clock mode: A power-saving operation mode in which only the clock count can operate simply at an oscillating clock of 32.768 kHz while the CPU is set to OFF.

Table 1 Examples of the Reduced Instruction Cycle

Example of reduced instruction cycle	F ² MC-8FX	F ² MC-8L
DIVU A	17 cycles (16-bit ÷ 16-bit)	21 cycles (16-bit ÷ 8-bit)
MULU A	8 cycles	19 cycles
ADDCW A	1 cycle	3 cycles
SUBCW A	1 cycle	3 cycles

Table 2 Clock Frequency and Gear Ratio

	F ² MC-8FX	F ² MC-8L
CPU maximum operating frequency	10MHz	3MHz
Minimum instruction cycle	100ns	333ns
Main clock gear function	32 frequency divisions 16 frequency divisions 8 frequency divisions 2 frequency divisions 1 multiplication 2 multiplications 2.5 multiplications	64 frequency divisions 16 frequency divisions 8 frequency divisions 4 frequency divisions
Sub-clock gear function	2 frequency divisions 4 multiplications	2 frequency divisions

Figure 3 F²MC-8FX Family Product Lineup Plan

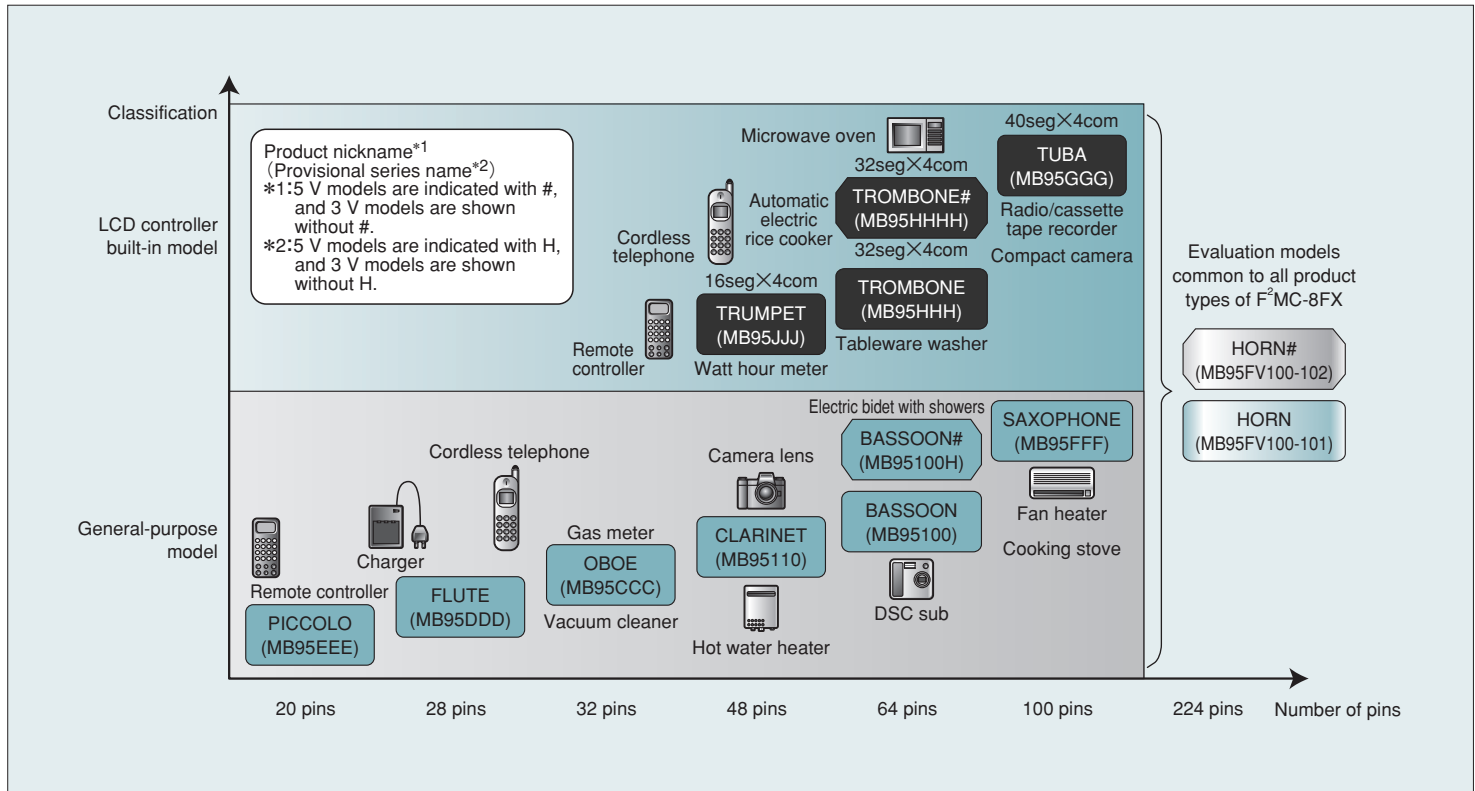


Figure 4 Conversion of Direct-Access Domain

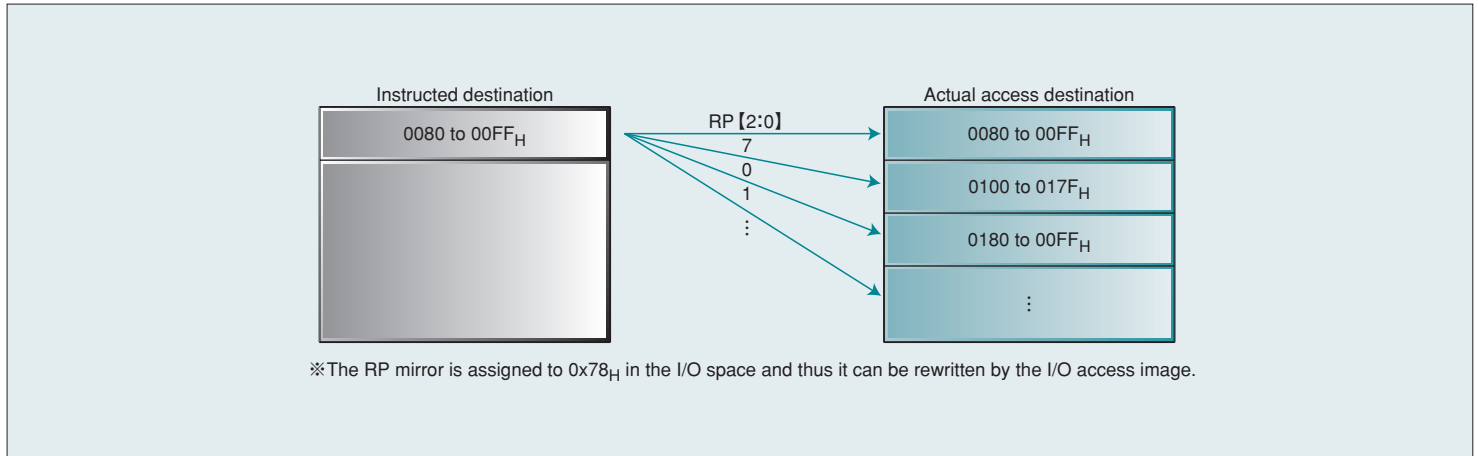


Figure 5 MB95100/H Series Block Diagram

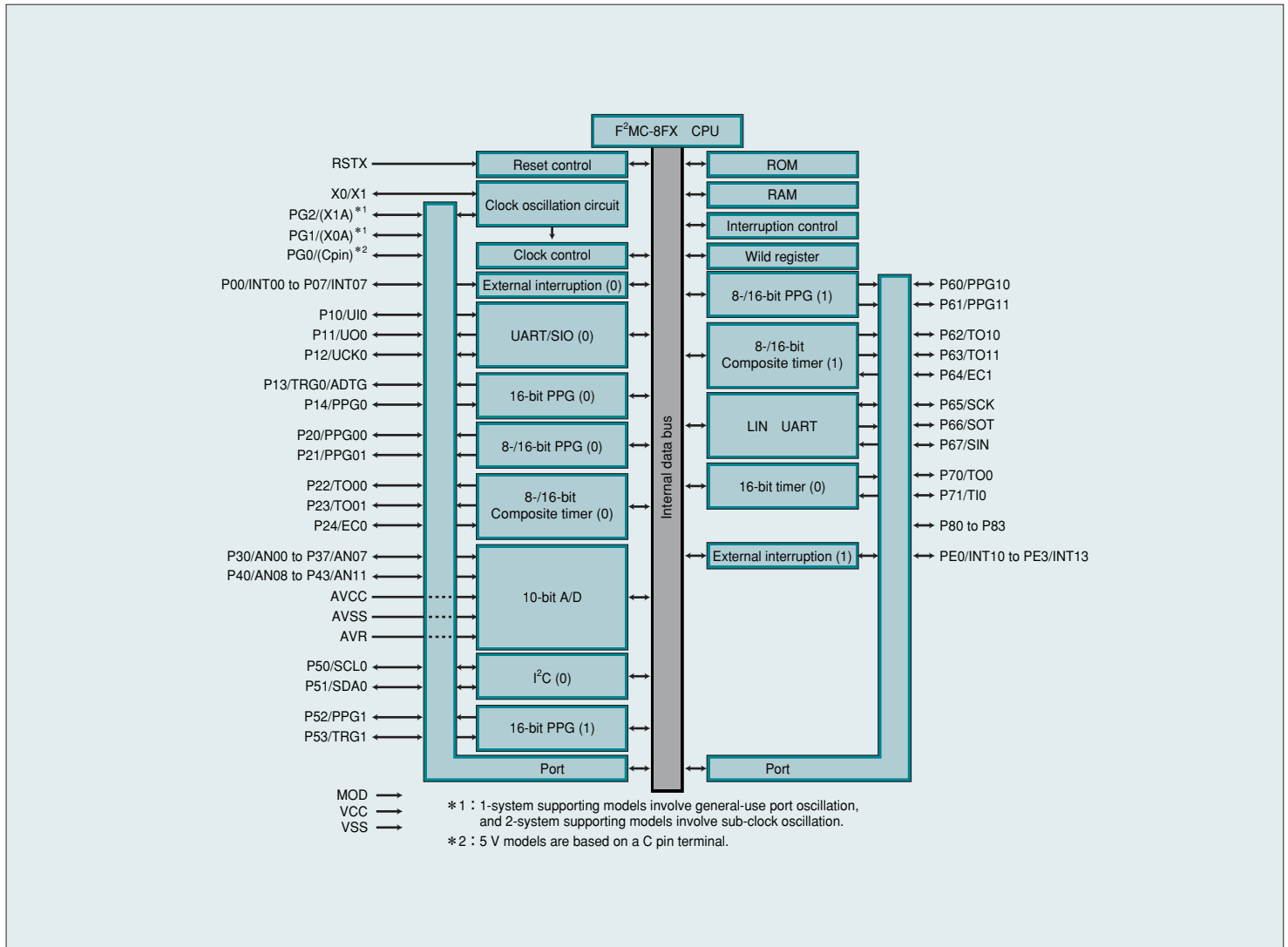


Figure 6 Block Diagram (MB95110)

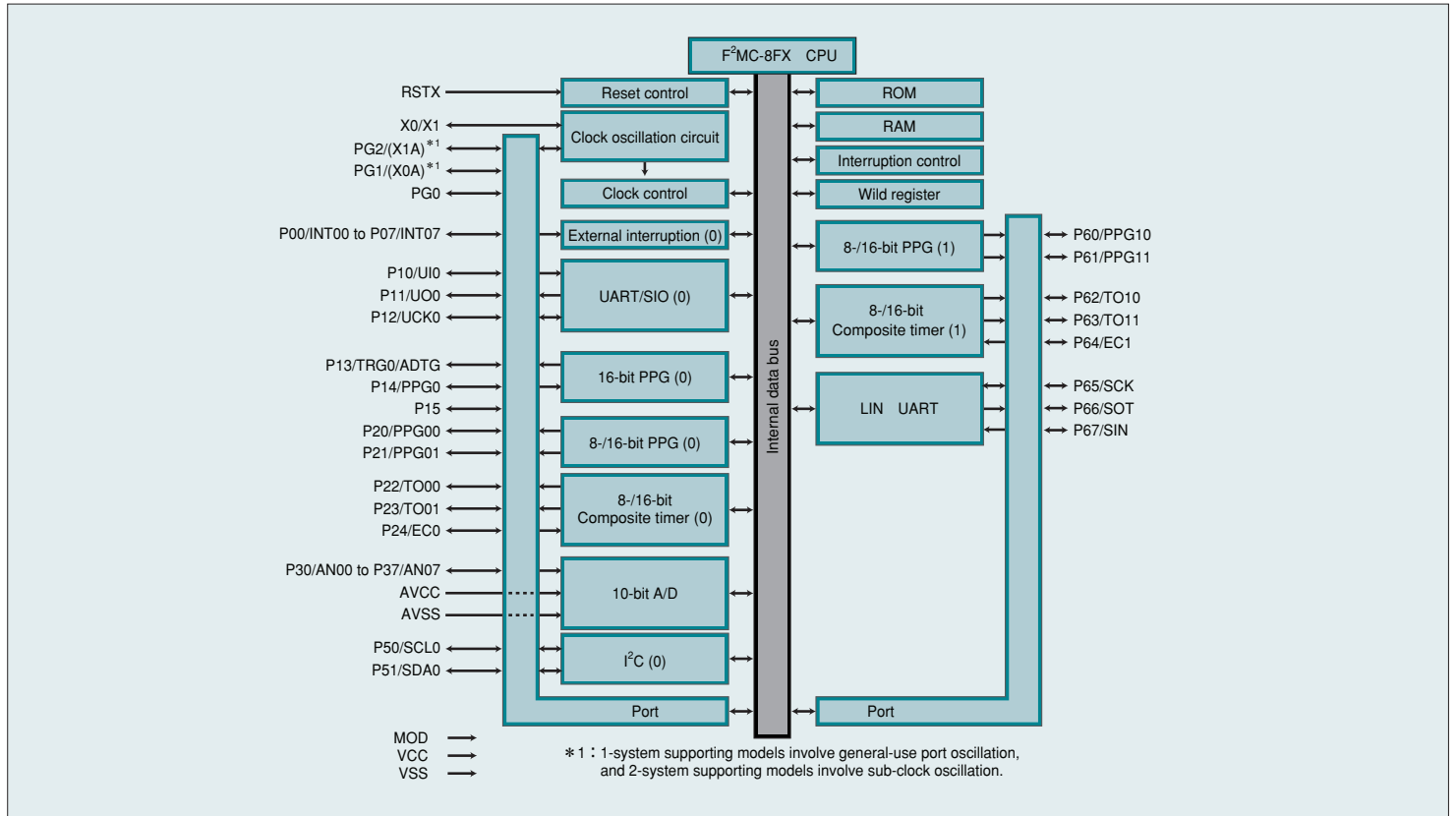


Figure 7 F²MC-8FX Family Development Environment Hardware Configuration Diagram

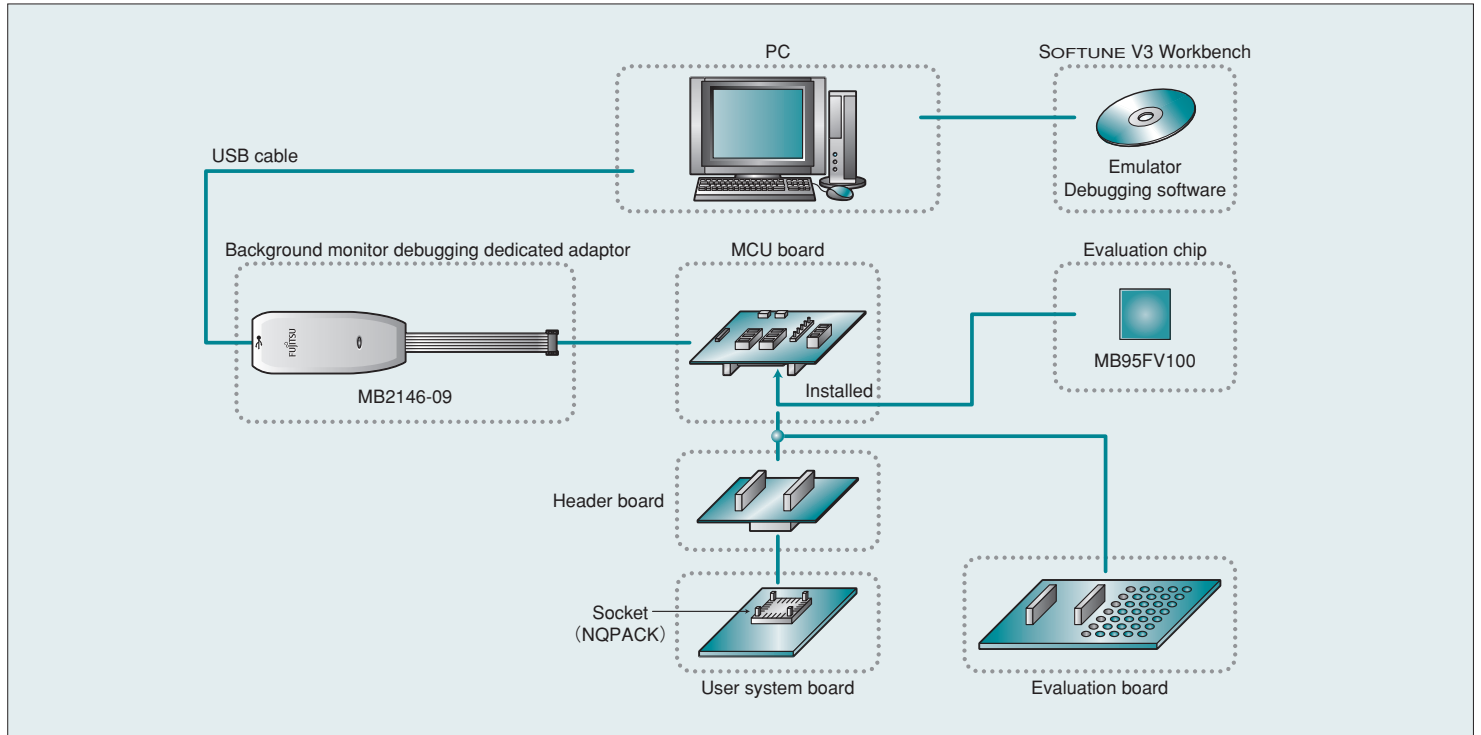


Table 3 Product Configuration and Available Functions

Item	Model	MB95100/H Series		MB95110 Series	
	MB95FV100	MB90F108/H (Under development)	MB95xxx/H (In planning)	MB95F118 (Under development)	MB95116 (In planning)
Class	For evaluation	Flash ROM	Mask ROM	Flash ROM	Mask ROM
ROM density	60K bytes	60K bytes	32K bytes to 60K bytes	60K bytes	32K bytes
RAM density	3.75K bytes	2K bytes	1K bytes to 2K bytes	2K bytes	1K bytes
CPU function	Number of basic instructions: 136 Data bit length: 1-, 8-, 16-bit length Minimum instruction execution time: 100 ns/10 MHz Maximum memory space: 64 Kbytes				
I/O port (max.)	89	55 (3 V, single-clock channel module) [Model name without H] 53 (3 V, 2-clock channel module) [Model name without H] 54 (5 V, single-clock channel module) [Model name with H] 52 (5 V, 2-clock channel module) [Model name with H]		40 (single-clock channel module) 38 (2-clock channel module)	
Time-base timer	Interruption interval at a 10 MHz main clock oscillation frequency: 0.2 ms, 1.64 ms, 6.6 ms, 52.4 ms				
Watchdog timer	Reset occurring interval at a 10 MHz main clock oscillation frequency (approx. 105 ms to 210 ms or approx. 210 ms to 419 ms) Reset occurring interval at a 32.768 KHz sub-clock oscillation frequency (approx. 250 ms to 500 ms or approx. 500 ms to 1 s)				
8-/16-bit composite timer	16-bit×2 channels (8-bit×4 channels)	16-bit×2 channels (8-bit×4 channels)		16-bit×2 channels (8-bit×4 channels)	
	Integrated with interval function, PWM function, PWC function, and input capture function.				
8-/16-bit PPG timer	16-bit×2 channels (8-bit×4 channels)	16-bit×2 channels (8-bit×4 channels)		16-bit×2 channels (8-bit×4 channels)	
	Allowable output of pulse waveform at any desired period and duty factor; Multiple channels can be simultaneously activated.				
16-bit PPG timer	3 channels	2 channels		2 channels	
	Allowable output of pulse waveform at any desired period and duty factor; Selective between PWM and one-shot modes; External trigger supported.				
16-bit reload timer	2 channels	1 channel		—	
	Selective among reload/one-shot/event counter modes; Allowable output of square waveform.				
Clock pre-scaler	Interval time with the sub-clock running at an oscillating frequency of 32.768 kHz: 125 ms, 250 ms, 500 ms, 1 s.				
Clock counter	A maximum of 63 clock counts available from the clock pre-scaler; Allowable 1-minute count.				
UART/SIO	2 channels	1 channel		1 channel	
	Either mode selective synchronous or asynchronous to clock; Built-in special baud rate generator.				
LIN UART	1 channel	1 channel		1 channel	
	Either mode selective synchronous, asynchronous, or LIN to clock; Built-in special baud rate generator.				
I ² C bus	2 channels	1 channel		1 channel	
	Compatible with Philips I ² C specifications; Master/slave transmission supported.				
A/D converter	16 channels	12 channels		8 channels	
	10-bit resolution; Selective between sampling and conversion time.				
External interruption	16 channels	12 channels		8 channels	
	The trigger mode is Rise edge, Fall edge, or both.				
Wild register	Allowable correction of a maximum of 6 bytes ROM data.				
LCD controller	40seg×4com	—			
Reset in response to any detected voltage drop	Optional (available with 5 V models); Unavailable with 3 V models.			—	
Clock supervisor	Optional (available with 5 V models); Unavailable with 3 V models.			—	
	Allowable supply of clock oscillated by the built-in CR to the CPU; Available switching to the built-in CR oscillation in response to detection of external oscillation shutdown.				
Power-saving mode	Stop mode/Sleep mode/Sub-clock mode/Clock mode				
Package	FBGA-224	LQFP-64 (0.5 mm pitch) LQFP-64 (0.65 mm pitch)		LQFP48 (0.5 mm pitch)	
Operating voltage	2.7V to 3.6V (3 V models) 3.0V to 5.5V (5 V models)	1.8V to 3.6V (3 V models) 2.2V to 5.5V (5 V models) [Target Spec]	1.8V to 3.6V (3 V models) 2.2V to 5.5V (5 V models) [Target Spec]		1.8V to 3.6V

Table 4 F²MC-8FX Family Development Tools List

Item		MB95100/H Series		MB95110 Series
		For LQFP64 0.5 mm pitch 10×10 mm	For LQFP64 0.65 mm pitch 12×12 mm	For LQFP48 0.5 mm pitch 7×7 mm
Hardware	Background monitor debugging dedicated adaptor	MB2146-09		
	Evaluation chip	MB95FV100-101 (intended specifically for 3 V products) MB95FV100-102 (intended specifically for 5 V products)		
	MCU board	Under development (configured with MB95FV100-101) Under development (configured with MB95FV100-102)		
	Header board for package conversion	Under development		
	Evaluation board	Under development		
Software		SOFTUNE V3 Workbench		
		SOFTUNE V3 C Compiler		
		SOFTUNE V3 Assembler		
		SOFTUNE V3 C Analyzer		
		SOFTUNE V3 C Checker		

Table 5 F²MC-8FX Family Development Tool Debugging Functions List

Adaptor model for debugging	MB2146-09
Host interface (download time)	USB: 12 Mbps (125 Kbps: at an operating frequency of 4 MHz)
Execution control	Continuous execution, step execution
Instruction execution break	256 points
Data break	2 points
Emulation memory	The size equivalent to Flash ROM MB95FV100 (60 K bytes)
Trace capacity	16 branches
Sequential break	2 levels (only code)