

F²MC-8L Family 8-bit LCDC Microcontrollers Configured with PLL Clock Multiplier Function for Sub Clock

MB89490 Series

MB89490 Series is a family of microcontrollers configured with a high-performance remote-control reception circuit and LCDC. The devices are best suited for compact disk controllers and other applications for mobile devices. The PLL clock multiplier circuit incorporated in the microcontrollers for the sub clocks effectively quadruples the operation speed compared to that of a conventional device.

Product Description

MB89490 Series is a lineup of single-chip microcontrollers operating on an F²MC-8L core with a high-performance remote-control reception circuit and LCDC. The devices are best suited for use as controllers for compact disk/cassette tape/radio receivers, compact cameras, mobile devices, and other applications. MB89490 lineup is also the first series of microcontrollers in the F²MC-8L LCDC-integrated family to be configured with built-in flash memories. The use of these new products for prototype development or initial mass production will enhance the efficiency of software development.

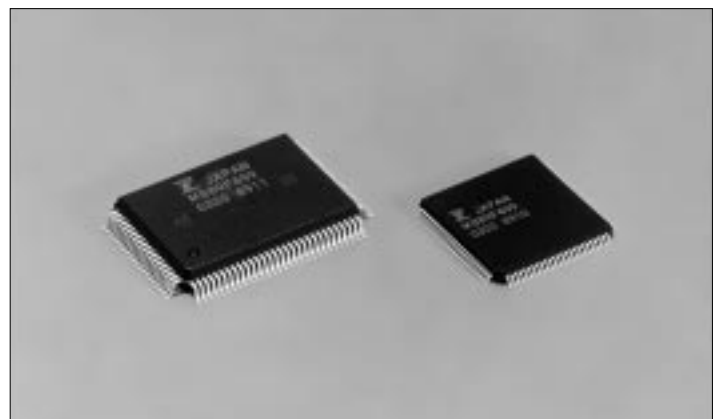
Product Features

■ High-speed operation available in the sub clock mode

The incorporated PLL clock multiplier circuit for the sub clock allows operation at a speed 4-times faster than that

attainable with the sub clock alone. The sub clock multiplier function sets the instruction execution cycle in the sub clock mode to $32.768\text{kHz} \times 4/2 = 65.536\text{kHz}$, assuring high-speed operation four times faster than that of earlier models in the

Photo 1 External View



F²MC-8L Family.

Remote-control reception becomes possible in the sub clock mode by delivering a series of 4-multiplied clock signals directly to the count clock in the remote-control reception circuit. The maximum clock frequency of the sub clock is 75kHz, and the maximum instruction execution cycle in the sub clock mode is 150kHz.

The use of the sub clock mode with the main clock set OFF helps reduce unwanted radiation noise.

■ Built-in high-performance remote-control reception circuit

The remote-control reception circuit allows noise elimination, 15-step FIFO for holding the pulse widths, and data evaluation based on the compare register. The combination of these three functions significantly reduces the software burden for processing remote-control reception.

The remote-control reception circuit in this Series can also be used as a PWC timer.

■ Integrated 3V single power supply flash memory

The flash memory incorporated in the MB89F499 microcontroller permits write/erase operations with a 3V single

power supply, thereby facilitating on-board programming/erase operations. The byte-by-byte programming capability also enables use of the device as an EEPROM substitute.

■ A variety of communication and timer functions

Communication function: UART/SIO: 1 channel, SIO: 1 channel, I²C: 1 channel

Timer: 8/16-bit timer/counter: 2 channels, 8-bit PWM timer: 2 channels, Time base timer, Clock timer, PWC timer (supported by the remote-control reception circuit)

■ Built-in LCD controller

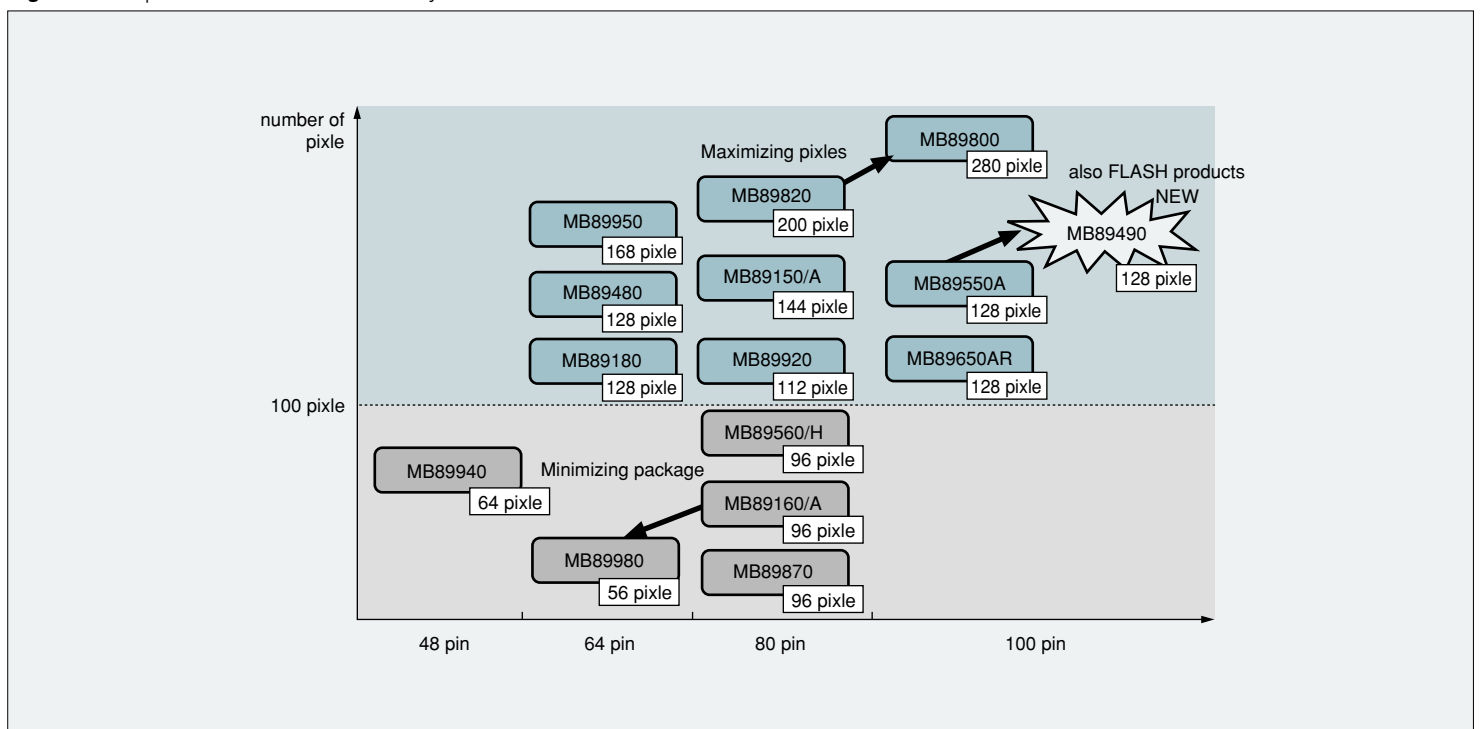
The LCDC allows 32 segments, 4 common output.

Fig. 1 shows lineup of Built-in LCD of F²MC-8L Family, **Fig. 2** shows the block diagram, **Table 1** the product lineup, **Table 2** the specifications.

Development Environment

This Series is supported by FUJITSU's integrated development environment SOFTUNE™ V3. SOFTUNE V3 features easy-to-use

Figure 1 Lineup of Built-in LCD of F²MC-8L Family



software developed to meet the diversified needs of program designers. The hardware is compatible with the F²MC Family emulator MB2140 Series that supports real-time debugging.

Table 3 lists the development tools and **Table 4** lists the writers supported by MB89F499. *

NOTES

* F²MC and SOFTUNE are registered trademarks of FUJITSU LIMITED.

Figure 2 Block Diagram

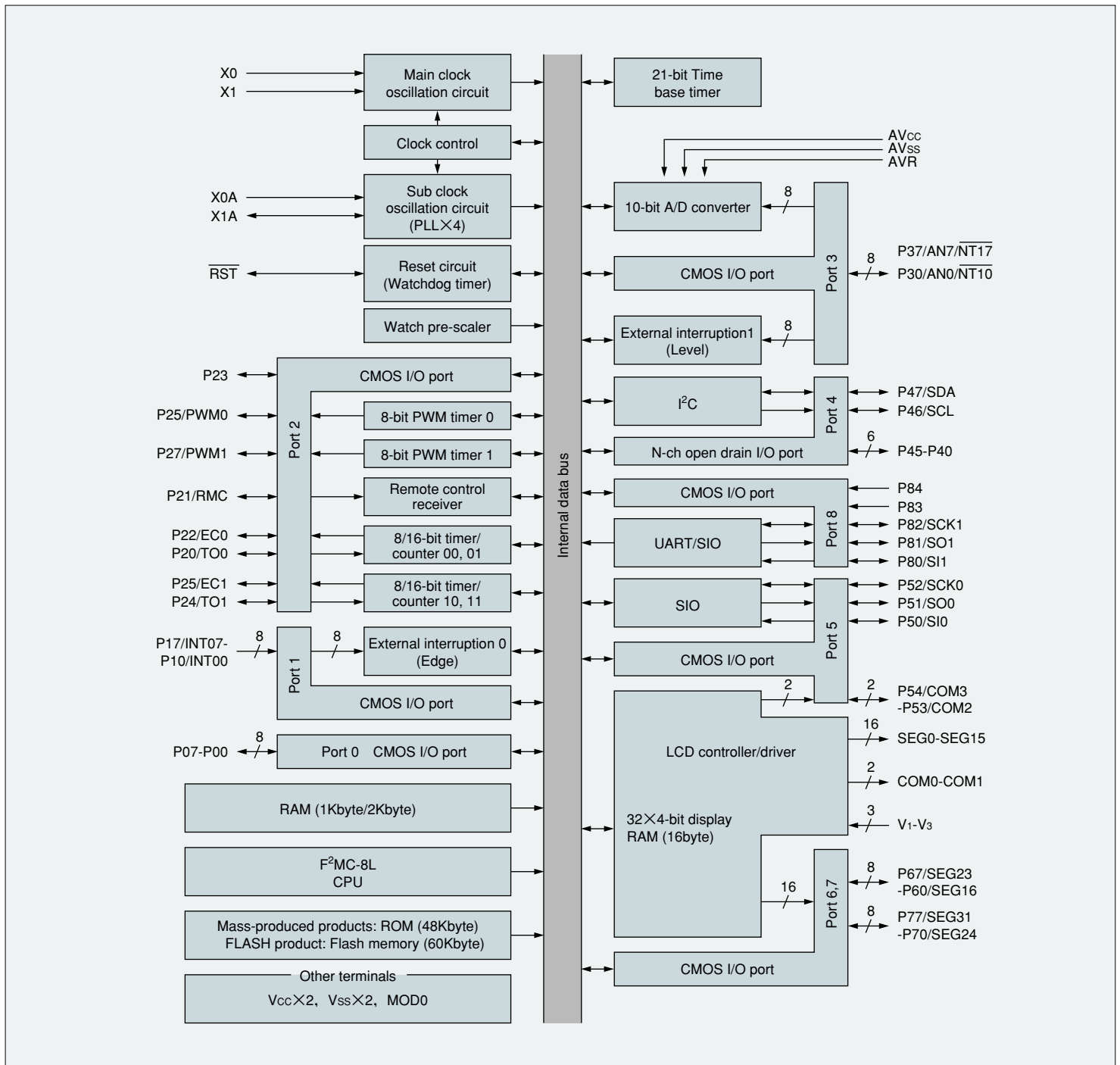


Table 1 Product Lineup

Device model	MB89498 (under development)	MB89F499	MB89PV490
Class	Mass-produced products (Mask ROM)	FLASH product	Piggyback & evaluation products/ For evaluation & development
ROM density	48Kbytes (Internal ROM)	60Kbytes (Built-in flash memory)	60Kbytes (External ROM)
RAM density	2Kbytes		
Low power consumption (Standby mode)	Sleep mode, Stop mode		
Process	CMOS		
Operating voltage	2.2V to 3.6V*	2.7V to 3.6V*	2.7V to 3.6V
Package	FPT-100P-M06 (QFP-100, 0.65mm) FPT-100P-M05 (LQFP-100, 0.5mm) under development		MQP-100C-P01 (MQFP-100, 0.65mm)

* The minimum operating voltage depends on the frequency used, functions used, and ICE connected.

Table 2 Specifications

Item	Specifications
CPU function	Number of basic instructions: 136 Instruction bit length: 8-bit Instruction length: 1 to 3bytes Data bit length: 1, 8, 16-bit length Minimum instruction execution time: 0.32 μ s to 5.12 μ s (@ an operating frequency of 12.5MHz) Interrupt processing time: 2.88 μ s to 46.08 μ s (@ an operating frequency of 12.5MHz)
Ports	I/O specific ports (CMOS): 56 Input specific ports (CMOS): 2 Nch open drain I/O ports: 8 Total: 66
Time base timer	21 bits Interruption interval: Main clock at 12.5MHz (About 0.655ms, 2.621ms, 20.97ms, 335.5ms)
Watchdog timer	Reset occurring interval: Main clock at 12.5MHz (167.8ms to 335.6ms) Reset occurring interval: Sub clock at 32.768kHz (500ms to 1000ms)
PWM timer	2 channels 8-bit interval timer operation (Available output of rectangular wave, Operation clock cycle: 1, 8, 16, 64T _{inst} *)
Clock pre-scaler	Interval time with the 17-bit sub clock running at an oscillating frequency of 32.768kHz (About 31.25ms, 0.25s, 0.50s, 1.00s, 4.00s)
8/16-bit timer/counter	2 channels 8-bit timer/counter operation executed by 2 channels(Timer 0 and Timer 1, each using an independent operation clock cycle), Alternatively, 16-bit timer/counter operation can be executed by 1 channel 16-bit event counter operation is used in the Timer 0 or 16-bit timer/counter operation (The trigger mode is either Rise edge or Fall edge, or both. Available output of lang1024 and square wave)
External interruption circuit 0	8 independent channels The trigger mode is either Rise edge or Fall edge, or both. Can be used for release from the standby mode.
External interruption circuit 1	8 independent channels, level detection functions Can be used for release from the standby mode.
A/D converter	10-bit resolution \times 8-channels Internal clock supports repetitive start Supply of reference voltage input (AVR)
LCD controller driver	Common output: 4 (Max.) Segment output: 32 (Max.) Power supply terminal (Bias): 3 (Max.) LCD display RAM capacity: 32 \times 4-bit
UART/SIO	CLK synchronous/CLK asynchronous data transmission possible (8-bit with parity bit, 9-bit without parity bit) Maximum baud rate: 97.656Kbps (@ 12.5MHz)
Serial I/O	8-bit length LSB first/MSB first selective Transfer clock (2, 8, 32T _{inst} *, external)
I ² C bus interface	1 channel 2-line type protocol used for communication with other devices
Remote control receiver circuit	15-step FIFO (number of interruption steps available for selection) for holding pulse width count values Noise elimination function Data evaluation function through compare register

* t_{inst}: Instruction cycle (execution time) Available selections: 1/4, 1/8, 1/16, 1/64 of main clock or 1/2, 2 of sub clock

Table 3 Development Tools

Hardware	Main unit MB2141A
	Emulation pod MB2144-508
	Probe cable MB2144-203
	Chip for development MB89PV490
	Evaluation board (Sunhayato Corporation) BBF2003-8L-100PS
Software	SOFTUNE V3 Workbench
	SOFTUNE V3 C Compiler
	SOFTUNE V3 Assembler
	SOFTUNE V3 C Analyzer
	SOFTUNE V3 C Checker

Table 4 Compatible Writers

Writer	Description
AF9708, AF9709 (Ando Electric Co., Ltd.)	General-purpose parallel writer
AF110, AF120, AF210, AF220 (Yokogawa Digital Computer Corporation)	General-purpose serial writer
PC serial writer (FUJITSU LIMITED)	Software allowing serial programming from PC through RS232C