

MB15FxxUL Series

Dual PLL Frequency Synthesizers with On-Chip Prescalers

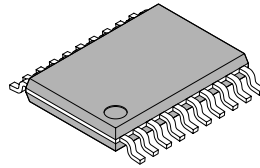
Description

The Fujitsu FxxSL series dual PLLs are serial input frequency synthesizers operating up to 6 GHz. They have built-in dual-modulus prescalers enabling pulse swallow operation. The latest advanced BiCMOS technology is used resulting in a super low supply current. A new charge pump design provides fast tuning along with low spurious noise and phase noise characteristics. The F-series is ideally suited for digital mobile communications, including GSM, DCS1800, PCS1900, IS-136, IS-95 and ISM applications. A new BCC-20 package decreases the mounting area by more than 30% over the older BCC-16 package.

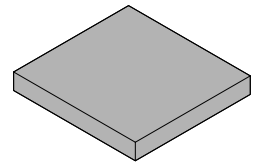
Features

- MB15F72UL and MB15F73UL: RF and IF PLLs
- MB15F74UL, MB15F76UL and MB15F78UL: Dual RF PLLs
- Very low spurious and phase noise characteristics
- Low operating voltage: 2.4 to 3.6 volts
- Low operating current: 2.5 to 9.0 mA (typical)
- Power-saving current: 0.1µA (typical)
- Wide operating temperature: -40 to +85°C
- Plastic 20-pin TSSOP and 20-pin BCC packages.
MB15F74 & 76UL available only in BCC package.
- Reference counter:
 - 14-bit programmable divider: 3 to 16383
- 18-bit programmable divider:
 - Binary 7-bit swallow counter: 0 to 127
 - Binary 11-bit programmable counter: 3 to 2047
- MB15F76UL
 - Binary 5-bit swallow counter: 0 to 31
 - Binary 13-bit swallow counter: 3 to 8191
- Software selectable charge pump current (± 1.5 or ± 6.0 mA)
- Evaluation Kits available

Packages



20-pin, Plastic TSSOP,
FPT-20P-M06



20-pad, Plastic BCC,
LCC-20P-M05

Parameter	MB15F72UL	MB15F73UL	MB15F74UL	MB15F76UL	MB15F78UL
RF Frequency of Operation, max.	1.3 GHz	2.25 GHz	4 GHz	6 GHz	2.6 GHz
IF/RF Frequency of Operation, max	350 MHz	600 MHz	2 GHz	1.5 GHz	1.2 GHz
Low Power Supply Voltage	2.7V	2.7V	2.7V	2.7V	2.7V
Low Power Supply Current	2.5 mA	3.2 mA	9.0 mA	9.0 mA	4.5 mA
Prescaler Divide Ratios	RF = 64/65 or 128/129, IF = 8/8 or 16/17		RF = 64/65 or 128/129 IF = 32/33 or 64/65	RF = 16/17, 32/33 & 1/4 IF = 4/5 or 8/9 & 1/4	RX = 32/33, 64/65 TX = 16/17, 32/33
Power-Saving Function	0.1µA typ.				

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MB15FxxUL Series

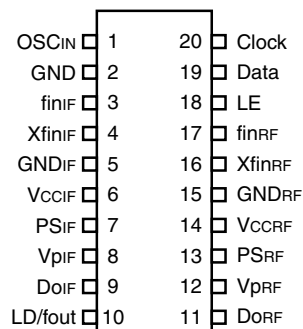
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Dual PLL Frequency Synthesizers with On-Chip Prescalers

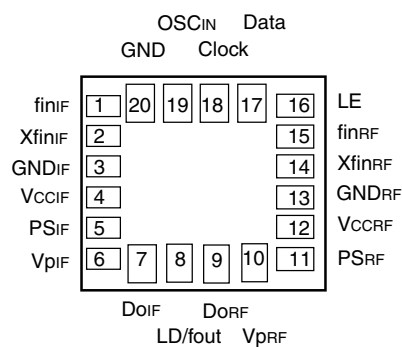
Pin Descriptions: MB15F72UL, MB15F73UL, MB15F74UL (BCC only), MB15F78UL

Pin No.		Pin Name	I/O	Descriptions
SSOP	BCC			
1	19	OSC _{IN}	I	The programmable reference divider input. TCXO should be connected with a AC coupling capacitor.
2	20	GND	–	Ground for OSC input buffer and the shift register circuit.
3	1	fin _{IF}	I	Prescaler input pin for the IF-PLL section. Connection to an external VCO should be AC coupling.
4	2	Xfin _{RF}	I	Prescaler complimentary input for the IF-PLL section. This pin should be grounded via a capacitor.
5	3	GND _{IF}	–	Ground for the IF-PLL section.
6	4	VCC _{IF}	–	Power supply voltage input pin for the IF-PLL section (except for the charge pump circuit), the shift register and the oscillator input buffer. When power is OFF, latched data of IF-PLL is lost.
7	5	PS _{IF}	I	Power saving mode control for the IF-PLL section. This pin must be set at "L" Power-ON. (Open is prohibited.) PS _{IF} = "H" ; Normal mode PS _{IF} = "L" ; Power saving mode
8	6	Vp _{IF}	–	Power supply voltage input pin for the IF-PLL charge pump.
9	7	Do _{IF}	O	Charge pump output for the IF-PLL section. Phase characteristics of the phase detector can be reversed by FC-bit.
10	8	LD/f _{OUT}	O	Lock detect signal output(LD)/ phase comparator monitoring output (fout). The output signal is selected by a LDS bit in a serial data. LDS bit = "1" ; outputs fout signal LDS bit = "0" ; outputs LD signal
11	9	Do _{RF}	O	Charge pump output for the RF-PLL section. Phase characteristics of the phase detector can be reversed by FC-bit.
12	10	Vp _{RF}	–	Power supply voltage input pin for the RF-PLL charge pump.
13	11	PS _{RF}	I	Power saving mode control for the RF-PLL section. This pin must be set at "L" Power-ON. (Open is prohibited.) PS _{RF} = "H" ; Normal mode PS _{RF} = "L" ; Power saving mode
14	12	VCC _{RF}	–	Power supply voltage input pin for the RF-PLL section (except for the charge pump circuit).
15	13	GND _{RF}	–	Ground for the RF-PLL section.
16	14	Xfin _{RF}	I	Prescaler complimentary input for the RF-PLL section. This pin should be grounded via a capacitor.
17	15	fin _{RF}	I	Prescaler input pin for the RF-PLL. Connction to an external VCO should be AC coupling.
18	16	LE	I	Load enable signal input (with the schmitt trigger circuit.) When LE is set "H", data in the shift register is transferred to the corresponding latch according to the control bit in a serial data.
19	17	Data	I	Serial data input (with the schmitt trigger circuit.) A data is transferred to the corresponding latch (IF-ref counter, IF-prog. counter, RF-ref. counter, RF-prog. counter) according to the control bit in a serial data.
20	18	Clock	I	Clock input for the 23-bit shift register (with the schmitt trigger circuit.) One bit data is shifted into the shift register on a rising edge of the clock.

Note: For F78UL IF=Tx, RF=Rx

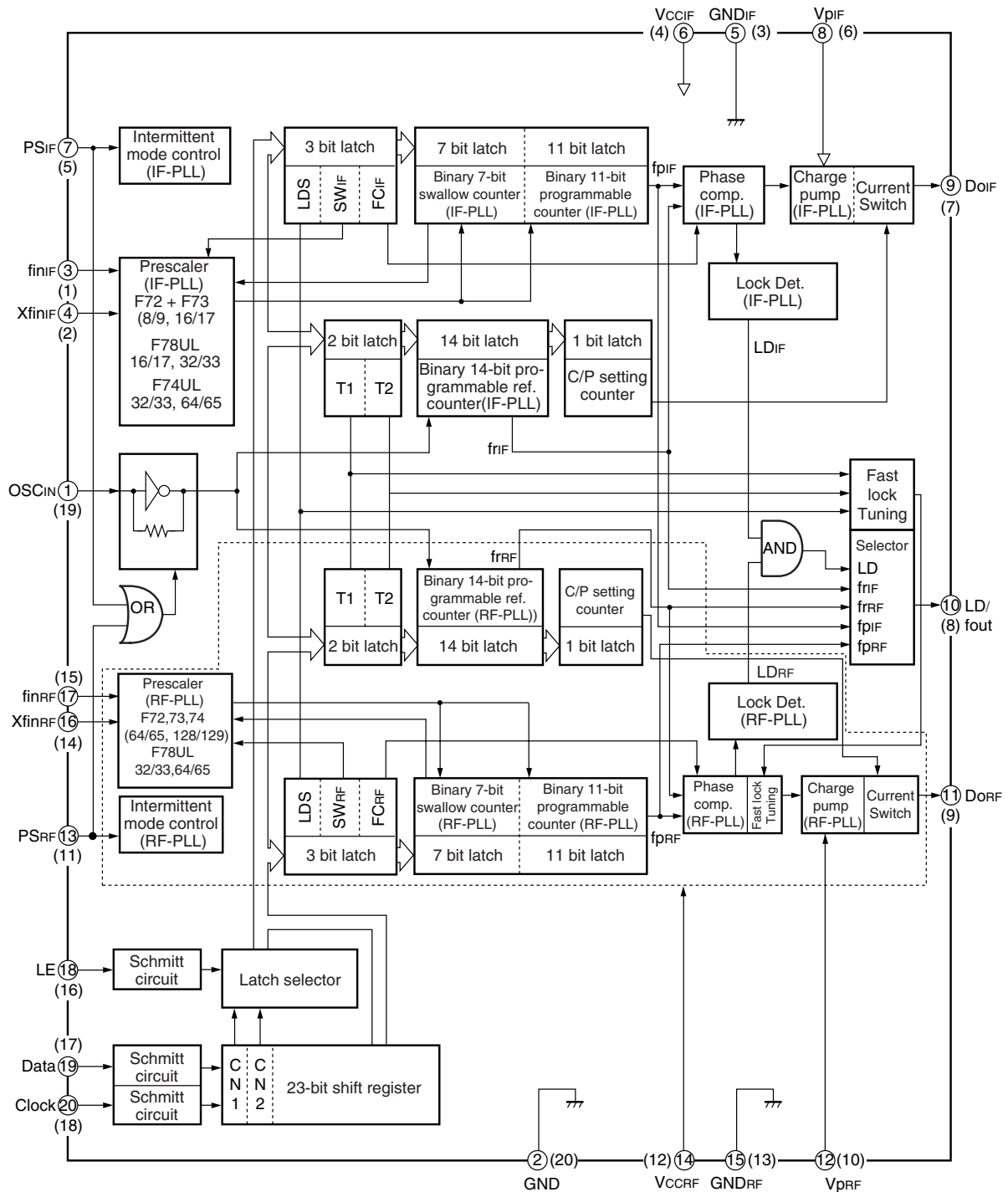


FPT-20P-M06



LCC-20P-M05

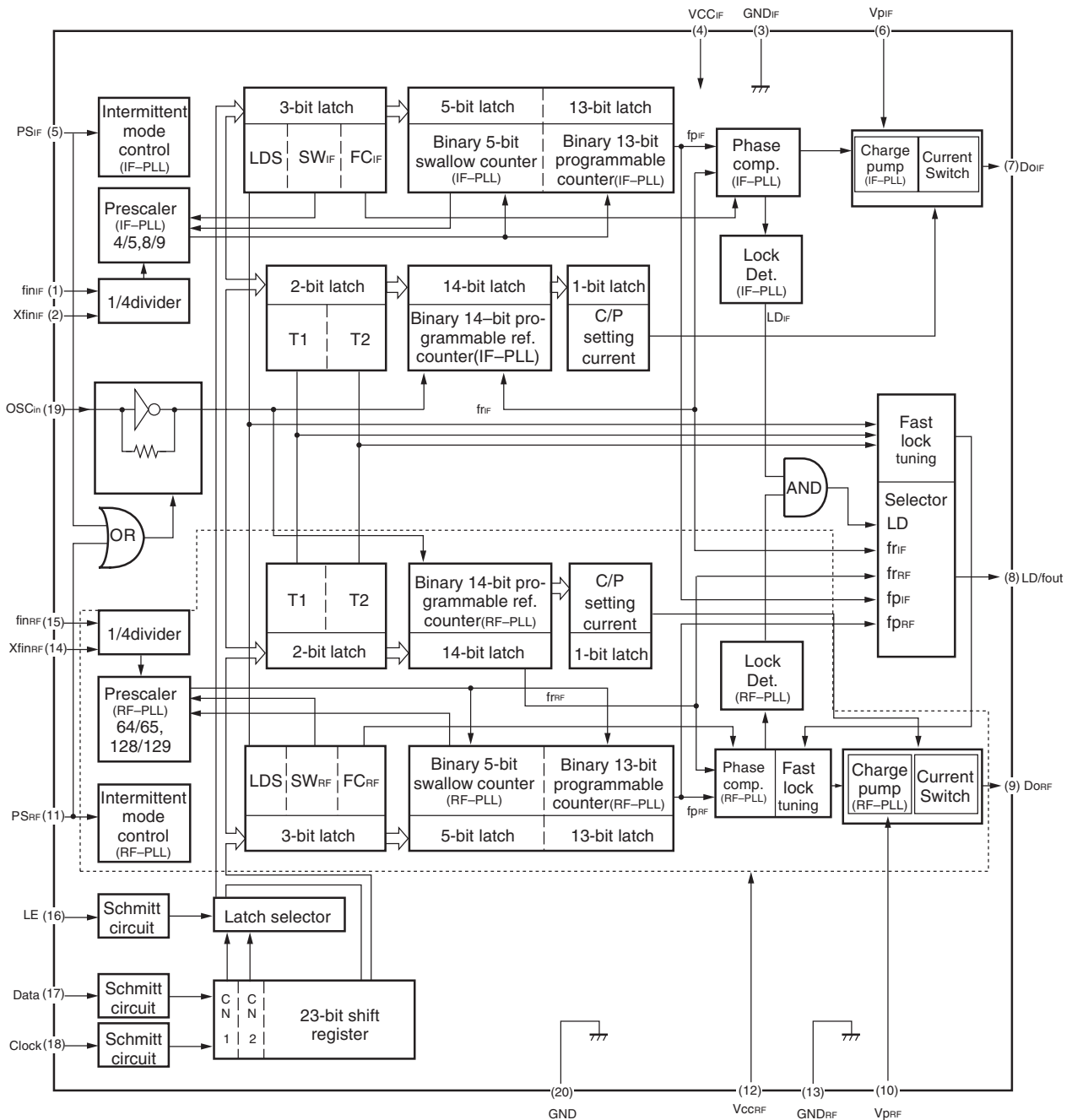
Block Diagram: MB15F72UL, MB15F73UL, MB15F74UL (BCC only), MB15F78UL



○ — TSSOP-20
 () — BCC 20
 Note: For F78UL IF=TX, RF=RX

Dual PLL Frequency Synthesizers with On-Chip Prescalers

Block Diagram: MB15F76UL (BCC Only)



Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Remark
Power supply voltage	V_{CC}	-0.5 to +4.0	V	
	V_P	V_{CC} to +4.0	V	
Input voltage	V_I	-0.5 to $V_{CC} + 0.5$	V	
Output voltage	V_O	GND to V_{CC}	V	LD/fout
	V_{DO}	GND to V_P	V	Do
Storage temperature	T_{STG}	-55 to +125	°C	

Note: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Value			Unit	Remark
		Min.	Typ.	Max.		
Power supply voltage	V_{CC}	2.4	2.7	3.6	V	$V_{CCRF} = V_{CCIF}$
	V_P	V_{CC}	2.7	3.6		
Input voltage	V_I	GND	-	V_{CC}	V	
Operating temperature	T_a	-40	-	+85	°C	

Handling Precautions

- V_{CCRF} , V_{PRF} , V_{CCIF} and V_{PIF} must supply equal voltage.
Even if either RF-PLL or IF-PLL is not used, power must be supplied to both V_{ccRF} , V_{pRF} , V_{ccIF} and V_{pIF} to keep them equal. It is recommended that the non-use PLL is controlled by power saving function.
- To protect against damage by electrostatic discharge, note the following handling precautions:
 - Store and transport devices in conductive containers.
 - Use properly grounded workstations, tools, and equipment.
 - Turn off power before inserting or removing this device into or from a socket.
 - Protect leads with conductive sheet, when transporting a board mounted device.

Warning: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the devices electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their Fujitsu representative beforehand.

Dual PLL Frequency Synthesizers with On-Chip Prescalers

Electrical Characteristics

Device Specifications

$V_{CC} = 2.4 \text{ to } 3.6 \text{ V, } T_a = -40 \text{ to } +85^\circ\text{C}$

Parameter	Symbol	MB15F72UL	MB15F73UL	MB15F74UL	MB15F76UL	MB15F78UL
Power supply current	$I_{CCIF, TX}^{*1}$	1.0 mA	1.2 mA	2.5 mA	2.0 mA	1.7 mA
	$I_{CCRF, RX}^{*1}$	1.5 mA	2.0 mA	6.5 mA	7.0 mA	2.8 mA
Power-saving current	I_{PSIF}^{*2}			0.1 μ A		
	I_{PSRF}^{*2}			0.1 μ A		
Operating frequency	f_{inIF}^{*3}	50 - 350 MHz	50 - 600 MHz	0.1 - 2 GHz	0.1 - 1.5 GHz	0.1 - 1.2 GHz
	f_{inRF}	0.1 - 1.3 GHz	0.2 - 2.25 GHz	2 - 4 GHz	2 - 6 GHz	0.4 - 2.6 GHz
	OSC_{in}^{*3}			3 - 40 MHz		

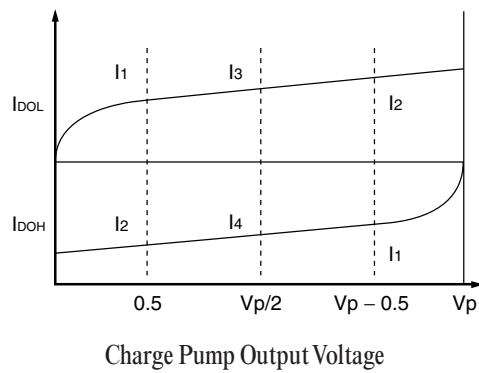
General Specifications

Parameter	Symbol	Condition	Value			Unit		
			Min.	Typ.	Max.			
Input sensitivity	$f_{inIF, PLL1}$	$Pf_{inIF, PLL1}$	50 Ω load system (Refer to measurement circuit)	-15	-	+2	dBm	
	$f_{inRF, PLL2}$	$Pf_{inRF, PLL2}$	50 Ω load system (Refer to measurement circuit)	-15	-	+2	dBm	
Input voltage	OSC_{in}	V_{OSC}		0.5	-	V_{CC}	V_{p-p}	
	Data, Clock, LE, PS	V_{IH} V_{IL}	-	$V_{CC} \times 0.7$ -	-	$V_{CC} \times 0.3$	V	
Input current	Data, Clock, LE, PS	I_{IH}^{*4} I_{IL}^{*4}	-	-1.0 -1.0	-	+1.0 +1.0	μ A	
	OSC_{in}	I_{IH} I_{IL}^{*4}	-	0 -100	-	+100 0	μ A	
		LD/ f_{OUT}	V_{OH} V_{OL}	$V_{CC} = 2.7V, I_{OH} = -1 \text{ mA}$ $V_{CC} = 2.7V, I_{OL} = 1 \text{ mA}$	$V_{CC} - 0.4$ -	-	0.4	V
Output voltage	Do	V_{DOH} V_{DOL}	$V_{CC} = 2.7V, I_{OH} = -0.5 \text{ mA}$ $V_{CC} = 2.7V, I_{OL} = 0.5 \text{ mA}$	$V_p - 0.4$ -	-	0.4	V	
		High impedance cutoff current	Do	I_{OFF}	$V_{CC} = 3.0V$ $V_{OFF} = .5V \text{ to } V_{CC} - 0.5V$	-	-	2.5
Output current	LD/ f_{out}	I_{OH}^{*4} I_{OL}	$V_{CC} = 2.7V$ $V_{CC} = 2.7V$	-1.0 -	-	-	1.0	mA
		Do ^{*8}	I_{DOH}^{*4}	$V_{CC} = 2.7,$ $V_{DOH} = V_{CC}/2,$ $T_a = +25^\circ\text{C}$	CS bit = "H" CS bit = "L"	-8.2 -2.2	-6.0 -1.5	-4.1 -0.8
	I_{DOL}		$V_{CC} = 3.0V,$ $V_{DOL} = V_{CC}/2,$ $T_a = +25^\circ\text{C}$	CS bit = "H" CS bit = "L"	4.1 0.8	6.0 1.5	8.2 2.2	mA
	Charge pump current characteristics	I_{DOL}/I_{DOH}	I_{DOMT}^{*5}	$V_{DO} = V_{CC}/2$	-	3	-	%
vs V_{DO}		I_{DOVD}^{*6}	$0.5V \leq V_{DO} \leq V_{CC} - 0.5V$	-	10	-	%	
vs T_a		I_{DOTA}^{*7}	$-40^\circ\text{C} \leq T_a \leq +85^\circ\text{C},$ $V_{DO} = V_{CC}/2$	-	5	-	%	

Note: See footnotes on the following page.

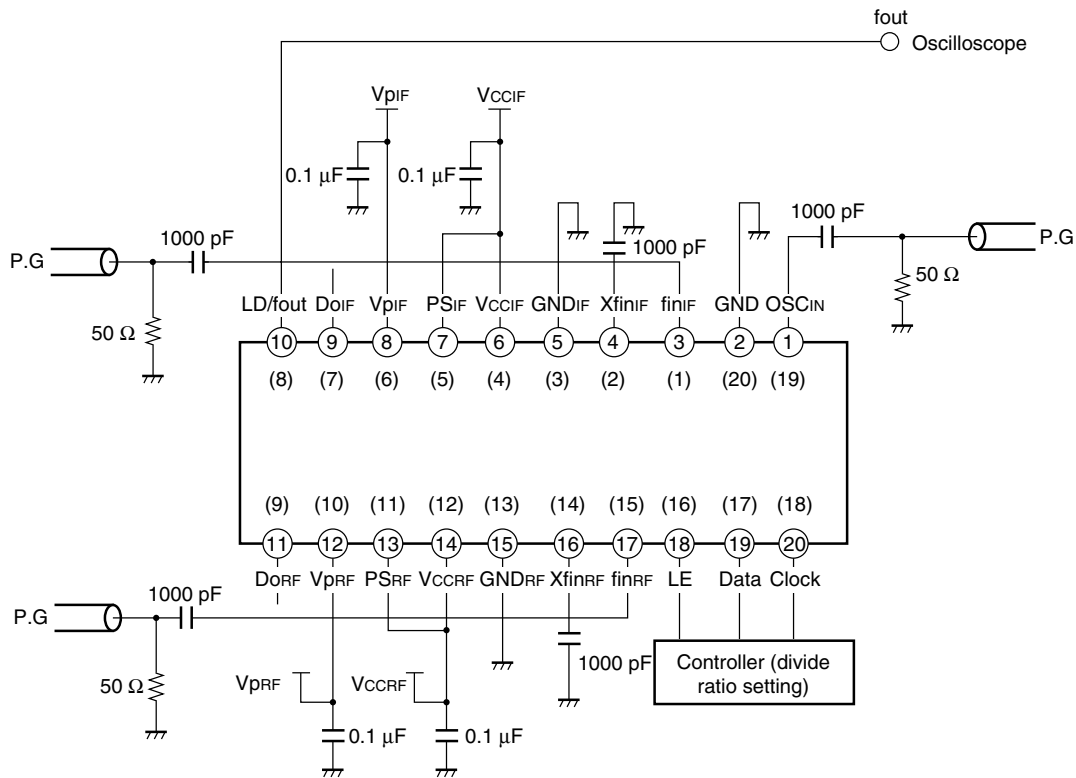
Electrical Characteristics

- *1 Conditions; fosc=12.8MHz, Ta = 25°C, SW="L" in locking state.
- *2 $V_{ccIF}=V_{pIF}=V_{ccRF}=V_{pRF}=2.7V$, fosc=12.8MHz, Ta = 25°C, in power saving mode.
- *3 AC coupling, 1000pF capacitor is connected under the condition of min. operating frequency.
- *4 The symbol "-" (minus) means direction of current flow.
- *5 $V_{cc}=V_p=2.7V$, Ta=25°C $(|I_{l3}| - |I_{l4}|) / [(|I_{l3}| + |I_{l4}|)/2] \times 100(\%)$
- *6 $V_{cc}=V_p=2.7V$, Ta=25°C $[(|I_{l2}| - |I_{l1}|) / 2] / [(|I_{l1}| + |I_{l2}|)/2] \times 100(\%)$ (Applied to each I_{DO(L)}, I_{DO(H)})
- *7 $V_{cc}=V_p=2.7V$, $[(|I_{DO(85C)}| - |I_{DO(-40C)}|) / 2] / [(|I_{DO(85C)}| + |I_{DO(-40C)}|) / 2] \times 100(\%)$ (Applied to each I_{DO(L)}, I_{DO(H)})
- *8 When Charge pump current is measured, set LDS="0", T1="0" and T2="1".
- *9 PS_{IF}=PS_{RF}=GND (V_{IL}=GND and V_{IH}=V_{cc} for Clock, Data, LE)



Dual PLL Frequency Synthesizers with On-Chip Prescalers

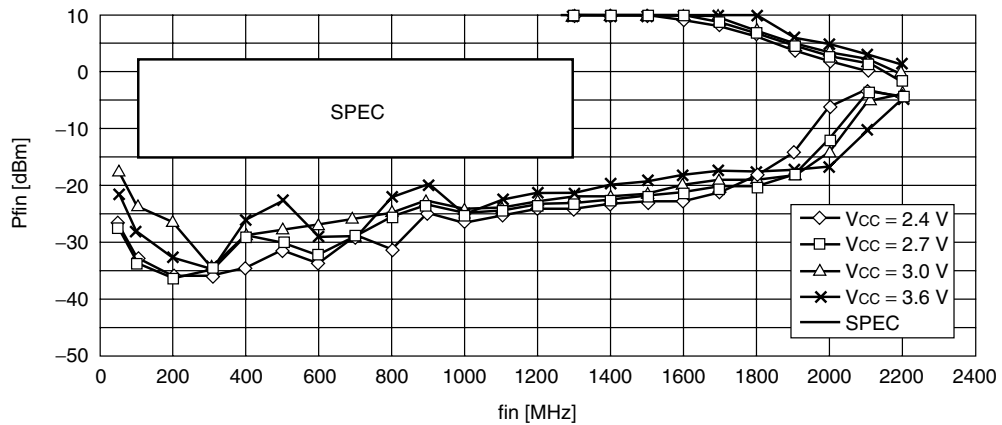
Test Circuit (For Measuring Input Sensitivity f_{IN}/OSC_{IN})



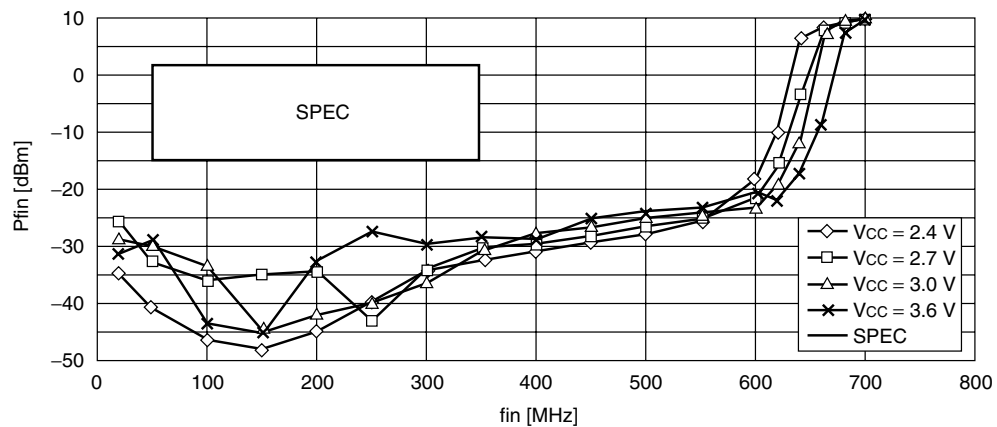
Note: ○ — TSSOP-20
 () — BCC 20

Typical Electrical Characteristics: MB15F72UL

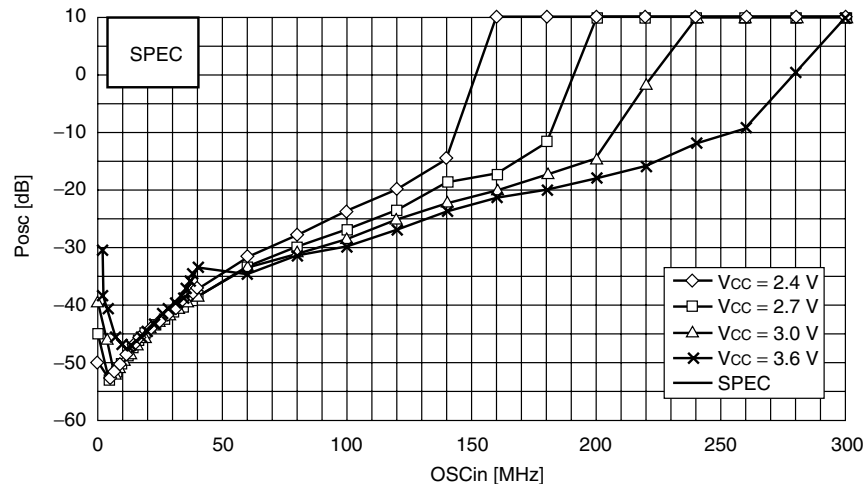
Input Sensitivity of f_{IN} RF Versus Input Frequency



Input Sensitivity of f_{IN} IF Versus Input Frequency



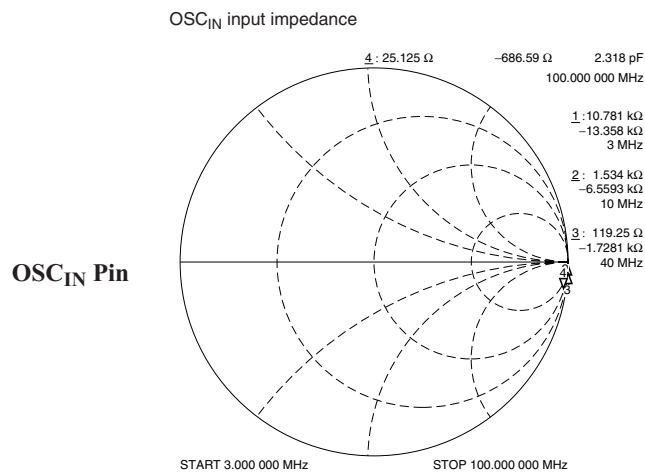
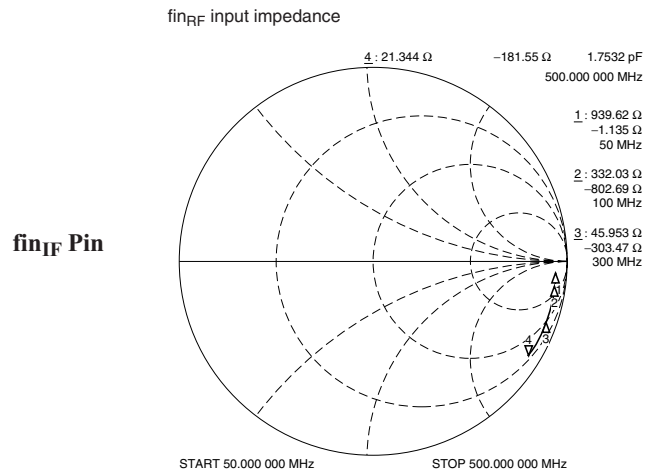
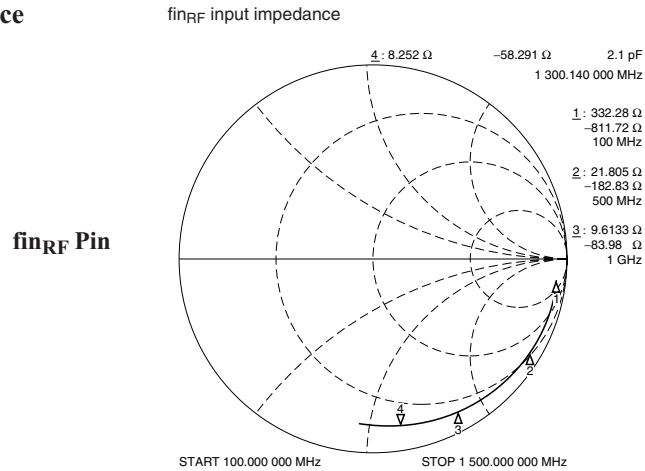
Input Sensitivity of OSC_{IN} Versus Input Frequency



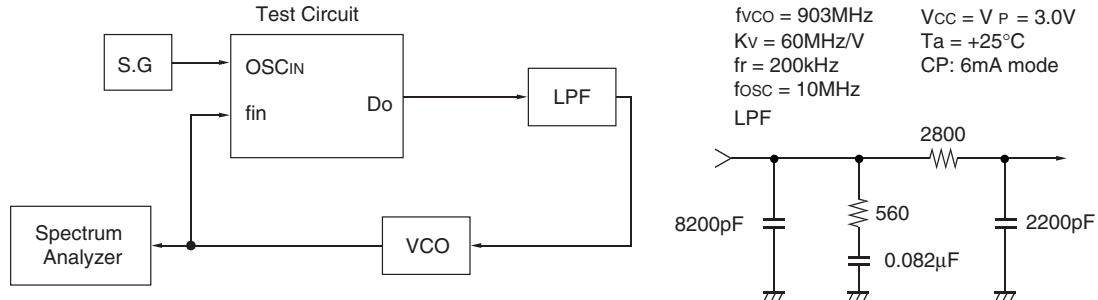
Dual PLL Frequency Synthesizers with On-Chip Prescalers

Typical Electrical Characteristics: MB15F72UL

Input Impedance

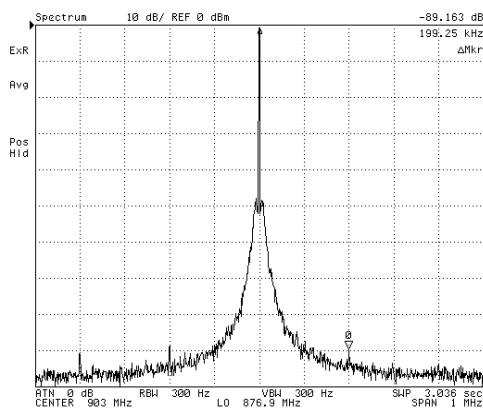


Reference Information: MB15F72UL

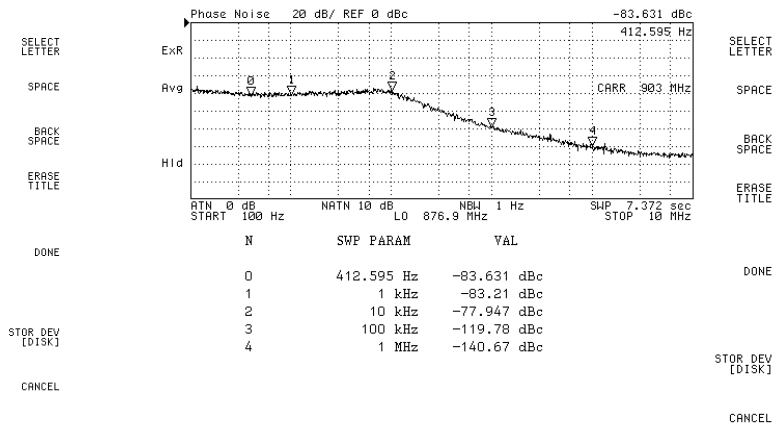


Typical plots measured with test circuit are shown below. The plots show lock up time, phase noise and reference leakage.

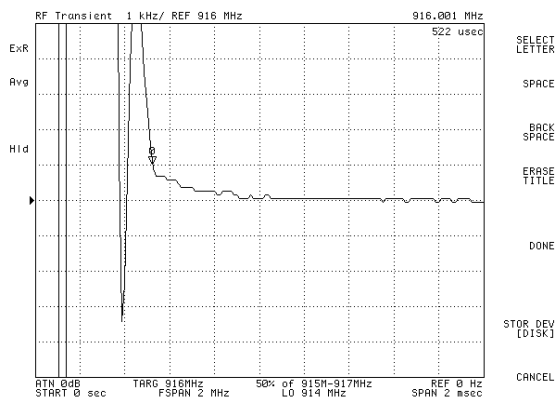
RF PLL Reference Leakage
@ 200 kHz offset = -89.1 dBc



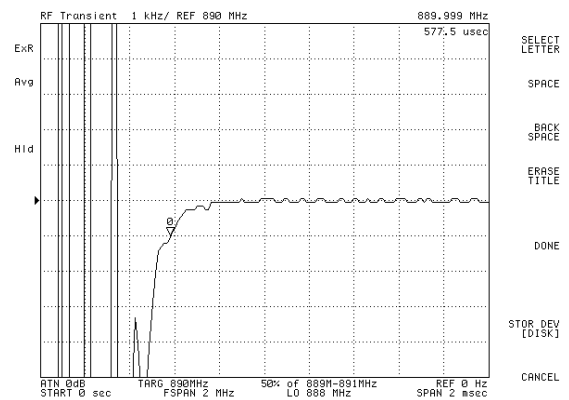
RF PLL Phase Noise
-83 dBc/Hz



RF PLL Lock Up Time = 522 μ s
890 MHz \rightarrow 916 MHz, within \pm 1kHz



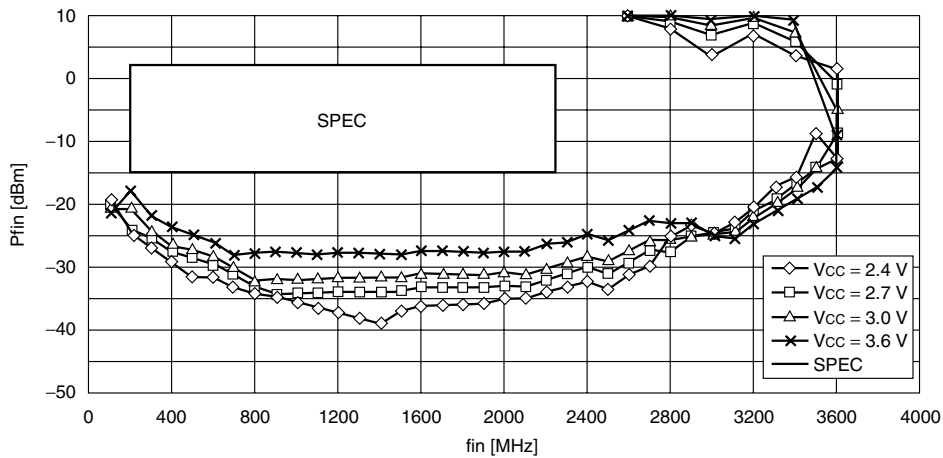
RF PLL Lock Up Time = 667 μ s
(916 MHz \rightarrow 890 MHz, within \pm 1kHz)



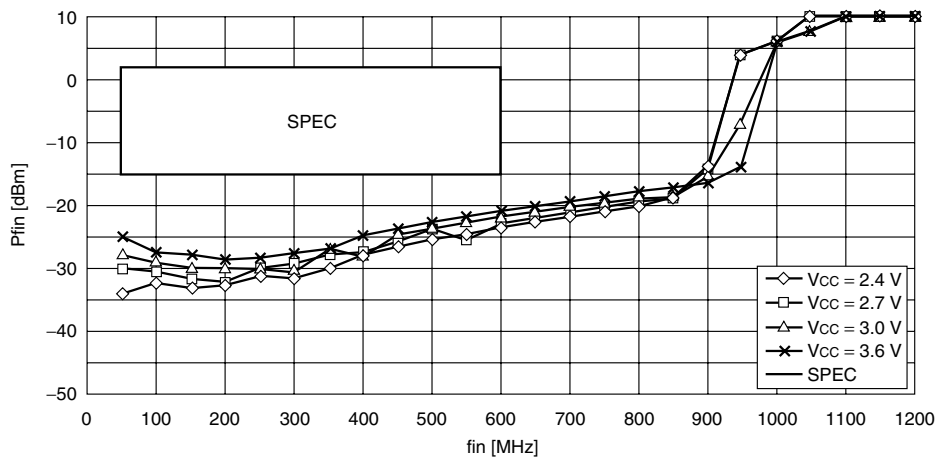
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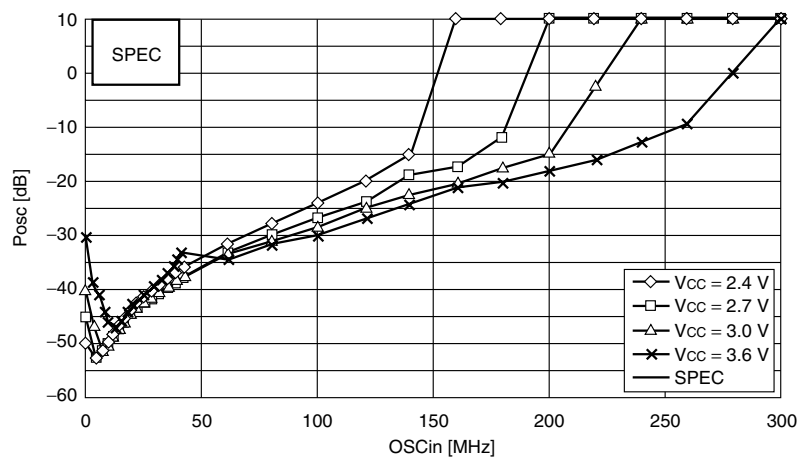
Input Sensitivity of RF f_{IN} Versus Input Frequency



Input Sensitivity of IF f_{IN} Versus Input Frequency

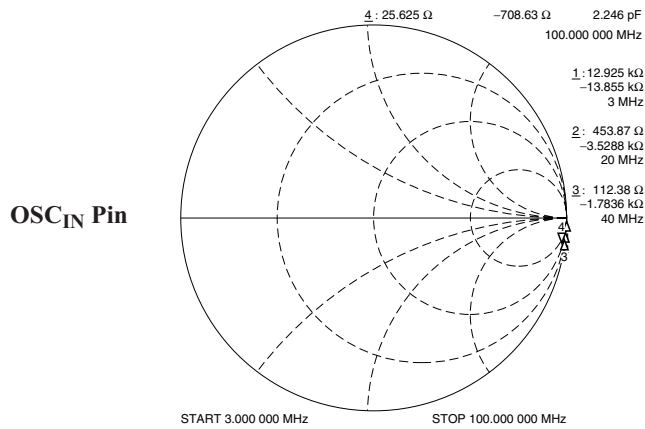
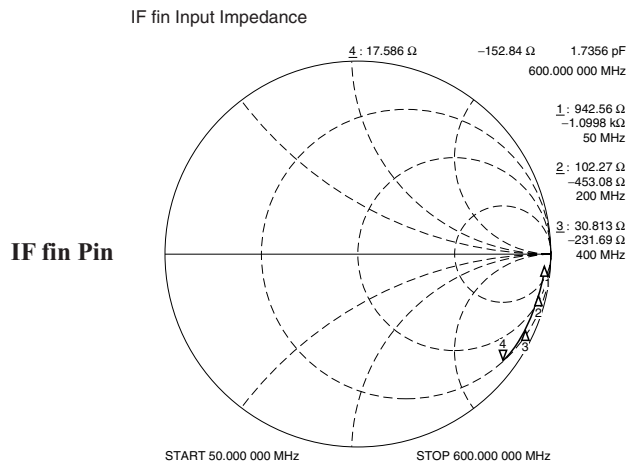
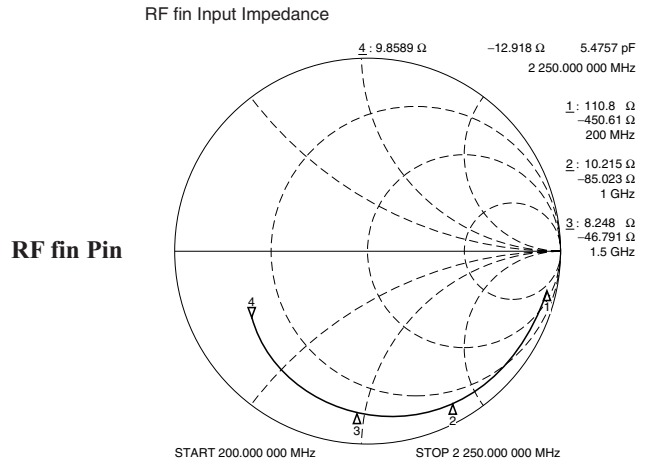


Input Sensitivity of OSC $_{IN}$ Versus Input Frequency



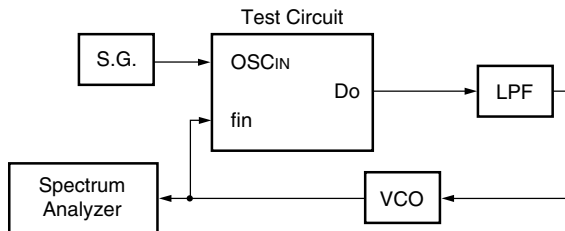
Typical Electrical Characteristics: MB15F73UL

Input Impedance

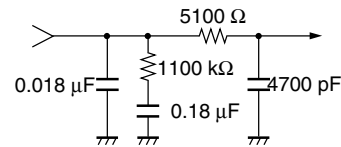


Dual PLL Frequency Synthesizers with On-Chip Prescalers

Reference Information: MB15F73UL

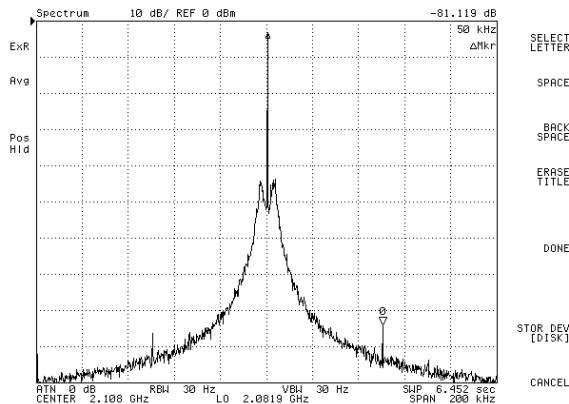


$f_{vco} = 2108\text{MHz}$ $V_{cc} = V_p = 3.0\text{V}$
 $K_v = 74\text{MHz/V}$ $T_a = +25\text{ }^\circ\text{C}$
 $f_r = 50\text{kHz}$ $CP : 6\text{mA mode}$
 $f_{osc} = 10\text{MHz}$
 LPF

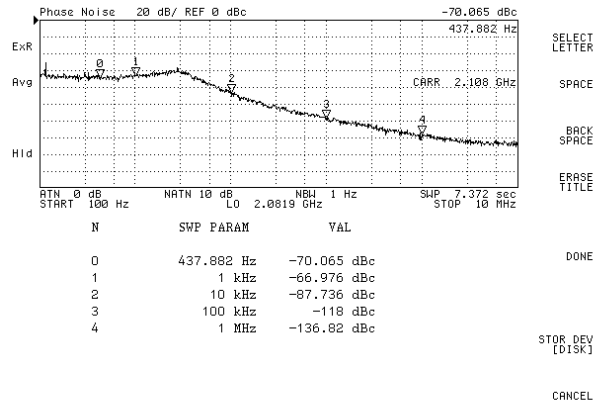


Typical plots measured with test circuit are shown below. The plots show lock up time, phase noise and reference leakage.

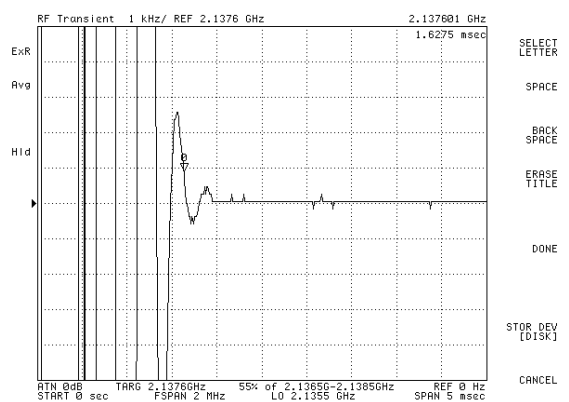
RF, PLL Reference Leakage
@ 50 kHz offset = -81.1 dBc



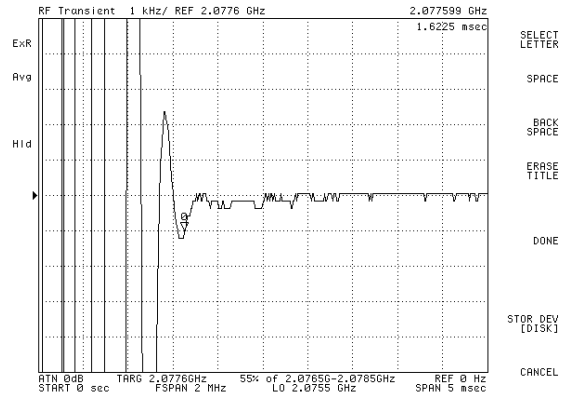
RF, PLL Phase Noise
-70.0 dBc/Hz



RF PLL Lock Up Time = 1.6msec
(2077.6 MHz → 2137.6 MHz, within ± 1kHz)

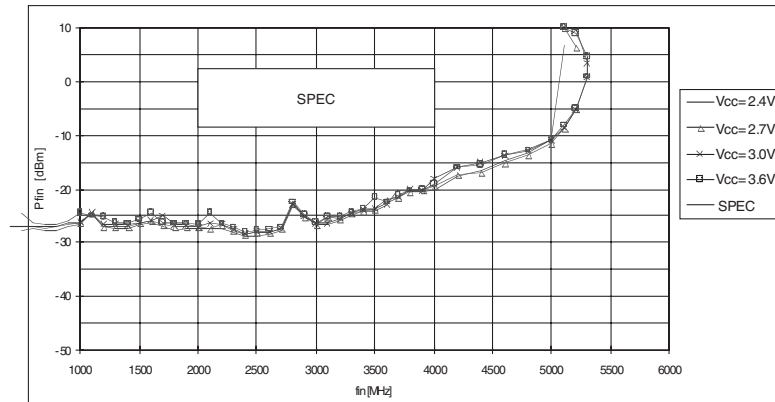


RF PLL Lock Up Time = 1.6msec
(2137.6 MHz → 2077.6 MHz, within ± 1kHz)

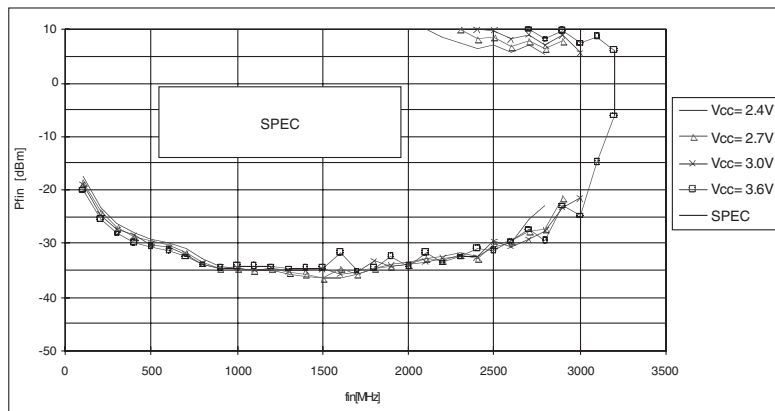


Typical Electrical Characteristics: MB15F74UL

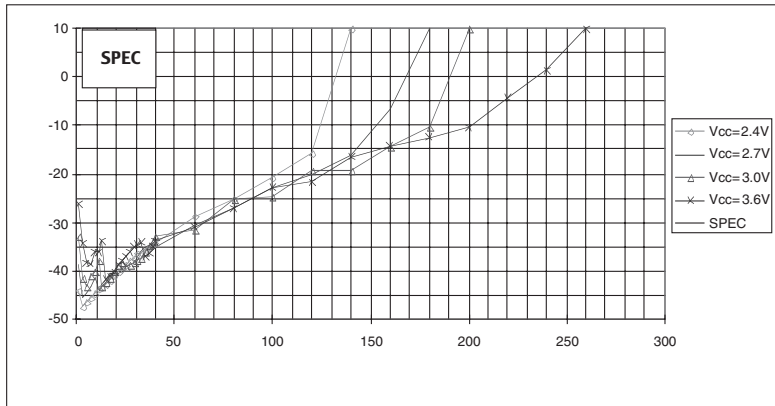
Input Sensitivity of f_{IN} RF Versus Input Frequency



Input Sensitivity of f_{IN} IF Versus Input Frequency



Input Sensitivity of OSC_{IN} versus Input Frequency



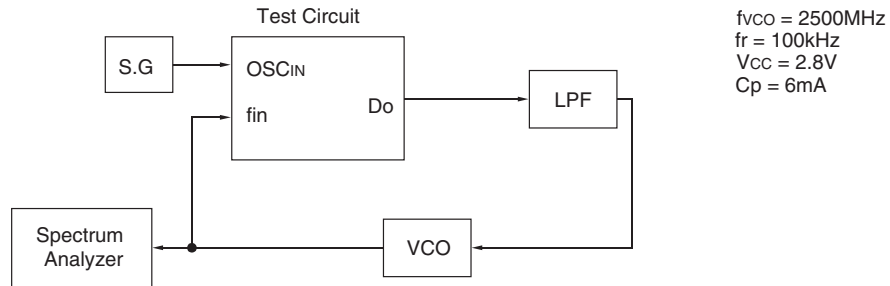
Dual PLL Frequency Synthesizers with On-Chip Prescalers

Typical Electrical Characteristics: MB15F74UL

Input Impedance

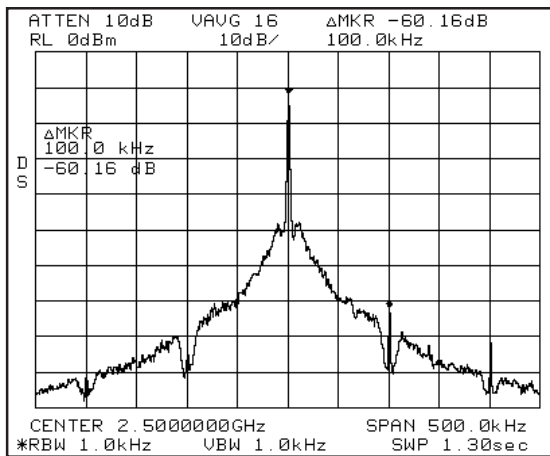
Contact Factory

Reference Information: MB15F74UL

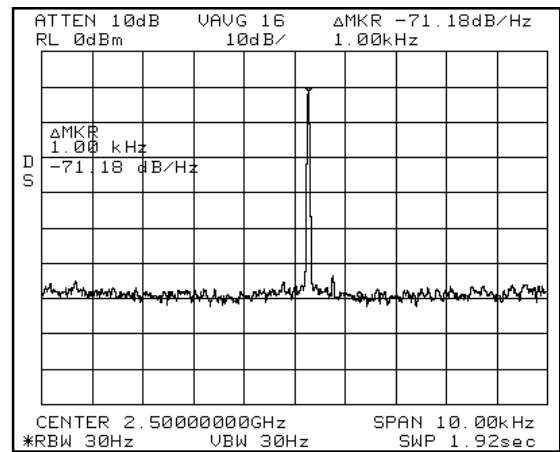


Typical plots measured with the test circuit are shown below. The plots show lock up time, phase noise and reference leakage.

RF PLL Reference Leakage
 @ 100 kHz offset = -60.1 dBc



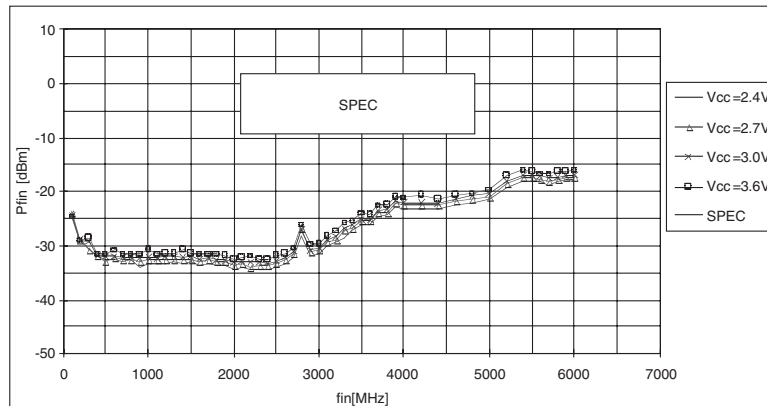
RF PLL Phase Noise
 @ max within loop band = -71.1 dBc/Hz



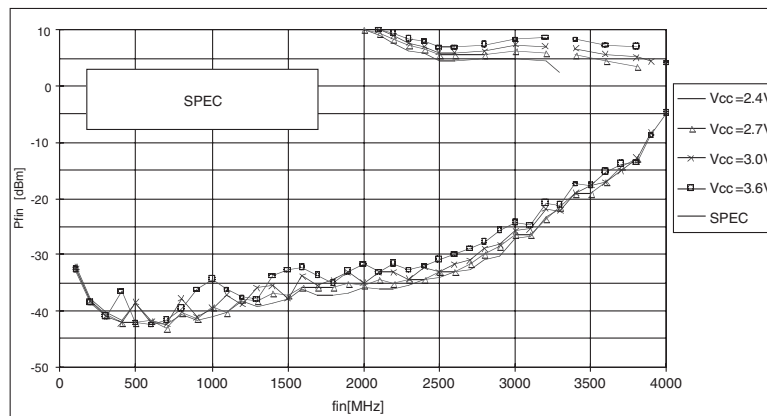
Dual PLL Frequency Synthesizers with On-Chip Prescalers

Typical Electrical Characteristics: MB15F76UL

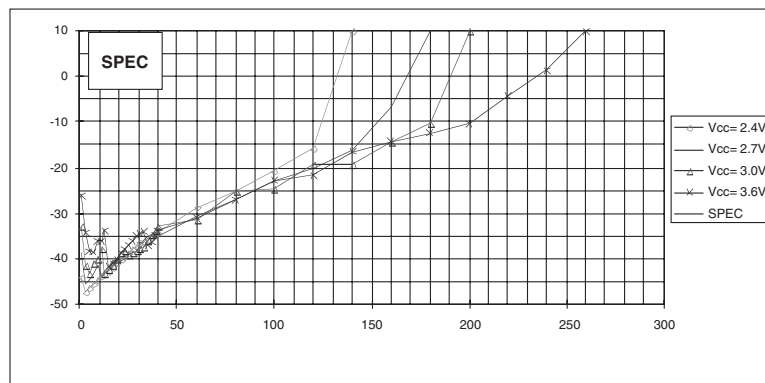
Input Sensivity of f_{IN} RF Versus Input Frequency



Input Sensivity of f_{IN} IF Versus Input Frequency



Input Sensivity of OSC_{IN} Versus Input Frequency



MB15FxxUL Series

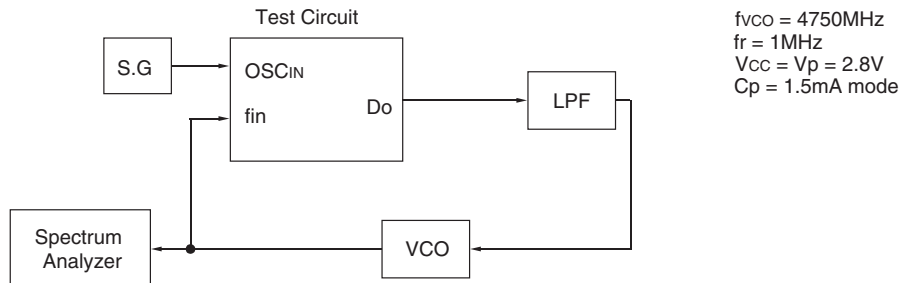
Typical Electrical Characteristics: MB15F76UL

Input Impedance

Contact Factory

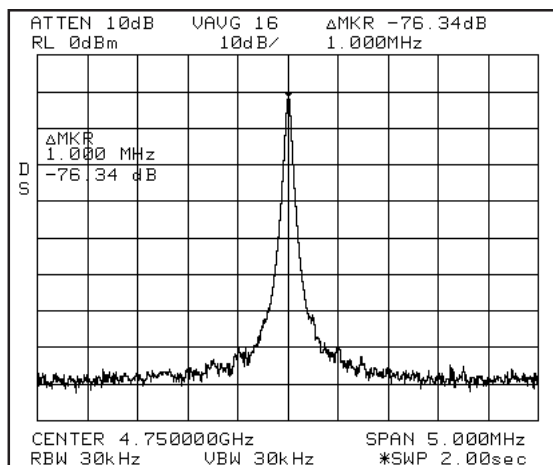
Dual PLL Frequency Synthesizers with On-Chip Prescalers

Reference Information: MB15F76UL

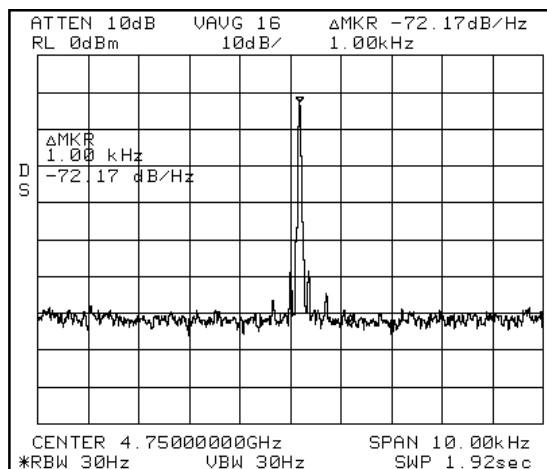


Typical plots measured with the test circuit are shown below. The plots show lock up time, phase noise and reference leakage.

RF PLL Reference Leakage
@ 1 MHz offset = -76.3 dBc

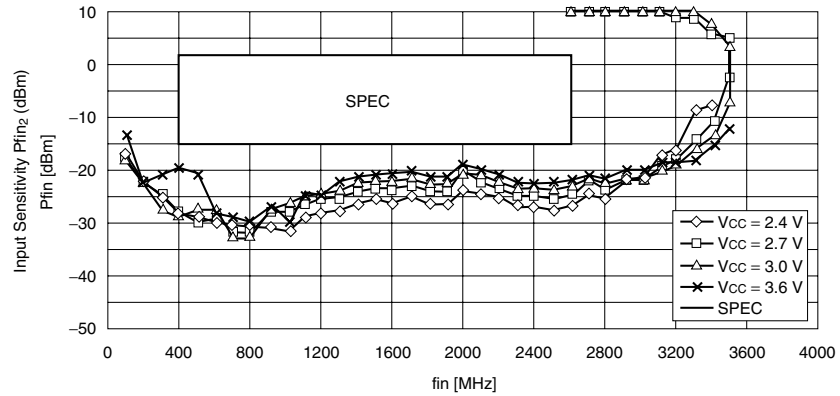


RF PLL Phase Noise
@ max within loop band = -72.17 dBc/Hz

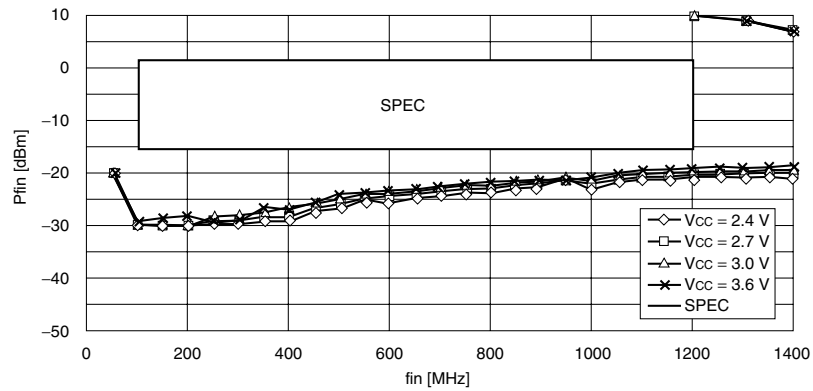


Typical Electrical Characteristics: MB15F78UL

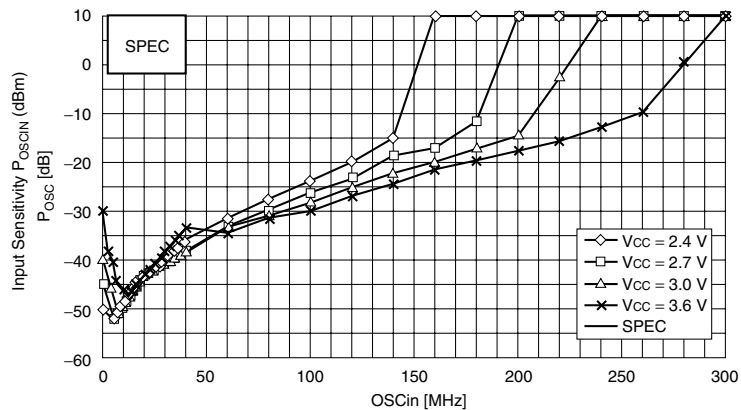
Input Sensivity of RX f_{IN} Versus Input Frequency



Input Sensivity of TX f_{IN} Versus Input Frequency



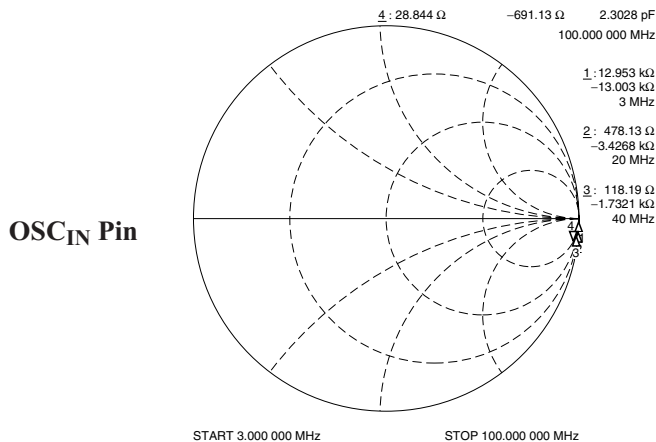
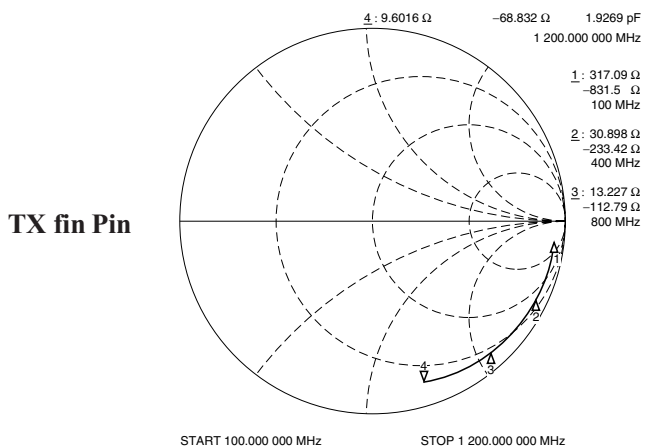
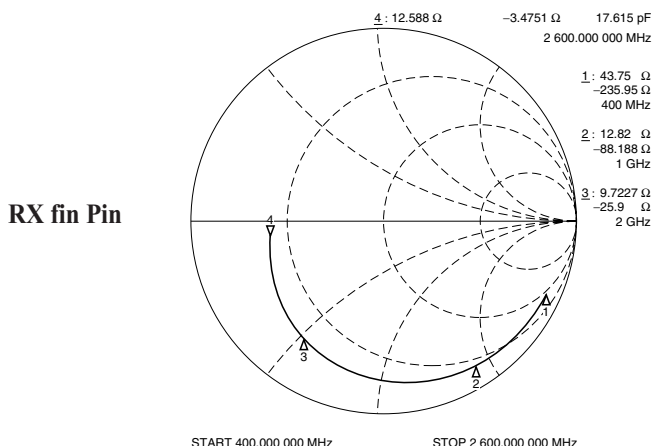
Input Sensivity of OSC_{IN} Versus Input Frequency



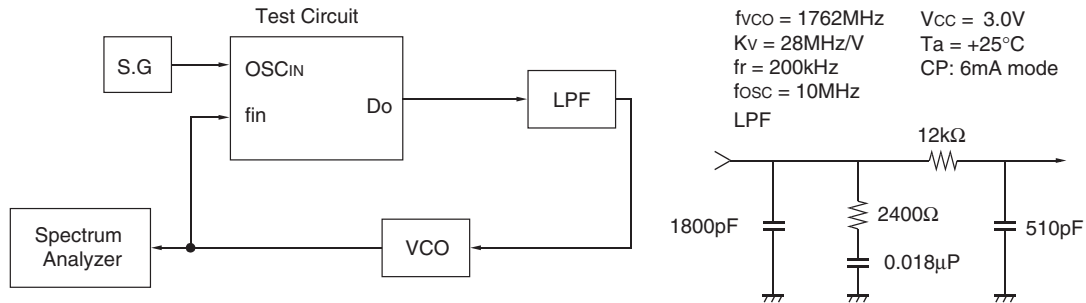
Dual PLL Frequency Synthesizers with On-Chip Prescalers

Typical Electrical Characteristics: MB15F78UL

Input Impedance

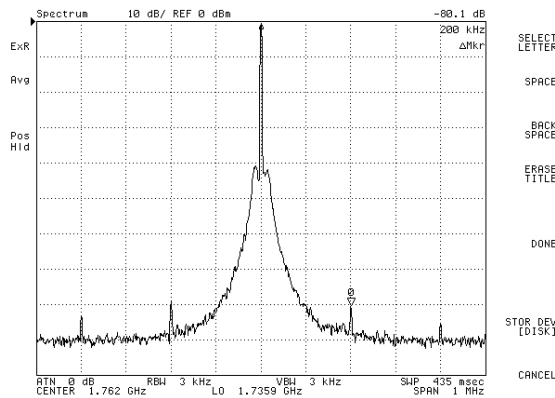


Reference Information: MB15F78UL

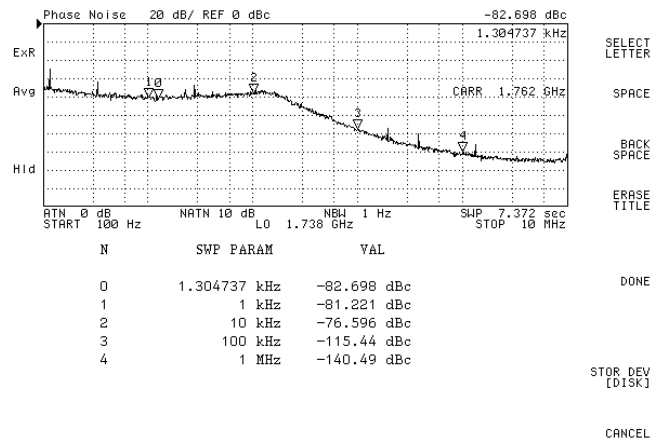


Typical plots measured with test circuit are shown below. The plots show lock up time, phase noise and reference leakage.

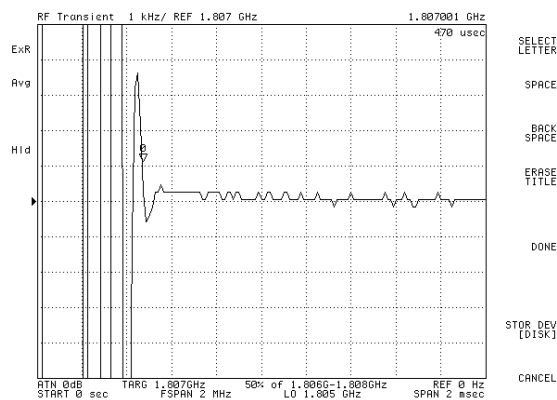
RX PLL Reference Leakage
@ 200 kHz offset = -80.1 dBc



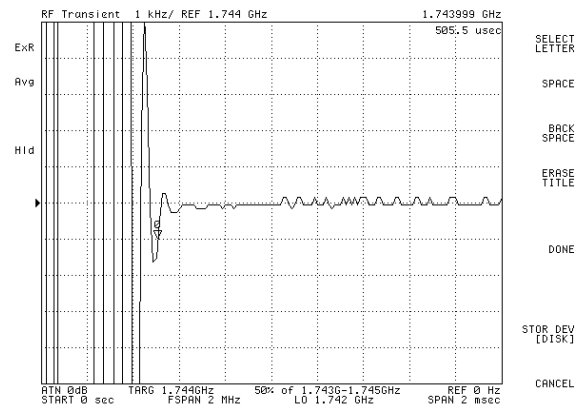
RX PLL Phase Noise
-82.6 dBc/Hz



RXPLL Lock Up Time = 470 μs
(1733.000 MHz → 1803.000 MHz, within ± 1kHz)



RX PLL Lock Up Time = 505 μs
(1803.000 MHz → 1733.000 MHz, within ± 1kHz)



Dual PLL Frequency Synthesizers with On-Chip Prescalers

Functional Descriptions

The VCO output frequency can be calculated using the following equation:

$$f_{VCO} = [(M \times N) + A] \times f_{OSC} \div R \quad (A < N)$$

- f_{VCO} Output frequency of external voltage controlled oscillator (VCO)
- M Preset divide ratio of dual modulus prescaler
- N Preset divide ratio of binary 11-bit programmable counter (3 to 2,047)
- A Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$)
- f_{OSC} Reference oscillation frequency
- R Preset divide ratio of binary 14-bit programmable reference counter (3 to 16,383)

For MB15F76UL Only

The divide ratio can be calculated using the equation:

$$f_{VCO} = [(PxN) + A] \times 4 \times f_{OSC} \div R$$

f_{VCO} : Output frequency of external voltage controlled oscillator (VCO)

- P: Preset divide ratio of dual modulus prescaler (4 or 8 for IF-PLL, 16 or 32 for RF-PLL)
- N: Preset divide ratio of binary 13-bit programmable counter (3 to 8,191)
- A: Preset divide ratio of binary 5-bit swallow counter ($0 \leq A \leq 31$, condition; $A < N$)
- f_{OSC} : Reference oscillation frequency
- R: Preset divide ratio of binary 14-bit programmable reference counter (3 to 16,383)

Serial Data Input

The serial data is entered using the Data, Clock and LE pins. The serial data controls the programmable reference counters and the programmable counters separately.

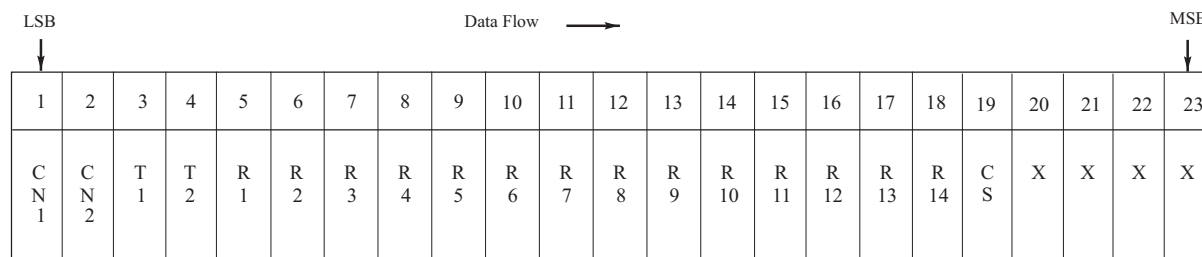
The binary serial data is entered through the Data pin when the LE pin is held low. One bit of data is shifted into the shift register on the rising edge of the Clock. When the LE signal pin is taken high, entered data is latched into the appropriate counters according to the control bit settings as follows:

Table 1. Control Bits

Control bit		Destination of serial data
CN1	CN2	
L	L	Programmable reference counter for IF-PLL or TX
H	L	Programmable reference counter for RF-PLL or RX
L	H	Programmable counter and swallow counter for IF-PLL or TX
H	H	Programmable counter and swallow counter for RF-PLL or RX

Shift Register Configuration

Programmable Reference Counter



- CNT1, 2 Control bits [Table 1]
- R1 to R14 Divide ratio setting bits for the programmable reference counter (3 to 16,383) [Table 2]
- T1, 2 Test purpose bits [Table 3]
- CS Charge pump current select bit [Table. 9]
- X Dummy bits(set "0" or "1")

Note: Input Data with MSB first.

Dual PLL Frequency Synthesizers with On-Chip Prescalers

Functional Descriptions

Table 4. Binary 11-Bit Programmable Counter Data Setting

Divide Ratio (N)	N 11	N 10	N 9	N 8	N 7	N 6	N 5	N 4	N 3	N 2	N 1
3	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	1	0	0
...
2047	1	1	1	1	1	1	1	1	1	1	1

Note: Divide ratio less than 3 is prohibited.

Table 4a. Binary 13-Bit Programmable Counter Data Setting (MB15F76UL only)

Divide Ratio (N)	N 13	N 12	N 11	N 10	N 9	N 8	N 7	N 6	N 5	N 4	N 3	N 2	N 1
3	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	1	0	0
...
8191	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: Divide ratio less than 3 is prohibited.

Table 5. Binary 7-Bit Swallow Counter Data Setting

Divide Ratio (N)	A 7	A 6	A 5	A 4	A 3	A 2	A 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
...
127	1	1	1	1	1	1	1

Note: Divide ratio (A) range = 0 to 127

Table 5a. Binary 5-Bit Swallow Counter Data Setting (MB15F76UL only)

Divide Ratio (N)	A 5	A 4	A 3	A 2	A 1
0	0	0	0	0	0
1	0	0	0	0	1
...
31	1	1	1	1	1

Note: Divide ratio (A) range = 0 to 31

Table 6. MB15F72UL Prescaler Data Setting

Prescaler Divide Ratio	SW = "H"	SW = "L"
IF-PLL	8/9	16/17
RF-PLL	64/65	128/129

MB15F73UL Prescaler Data Setting

Prescaler Divide Ratio	SW = "1"	SW = "0"
IF-PLL	8/9	16/17
RF-PLL	64/65	128/129

MB15F74UL Prescaler Data Setting

Prescaler Divide Ratio	SW = "1"	SW = "0"
IF-PLL	32/33	64/65
RF-PLL	64/65	128/129

MB15F76UL Prescaler Data Setting

Prescaler Divide Ratio	SW = "1"	SW = "0"
IF-PLL	4/5	8/9
RF-PLL	16/17	32/33

MB15F78UL Prescaler Data Setting

Prescaler Divide Ratio	SW = "1"	SW = "0"
TX-PLL	16/17	32/33
RX-PLL	32/33	64/65

Dual PLL Frequency Synthesizers with On-Chip Prescalers

Functional Descriptions

Table 7. Phase Comparator Phase Switching Data Setting

	$FC_{IF/PLL1,RF/PLL2} = H$	$FC_{IF/PLL1,RF/PLL2} = L$
	$DO_{IF/PLL1,RF/PLL2}$	
$f_r > f_p$	H	L
$f_r = f_p$	Z	Z
$f_r < f_p$	L	H
VCO polarity	(1)	(2)

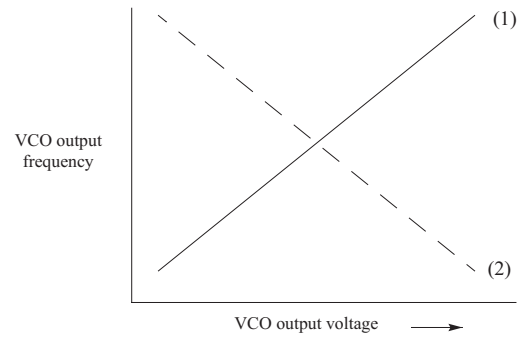
Notes: Z = High-impedance
FC bit should be set depending upon VCO and LPF polarity

Table 8. LD/f_{OUT} Output Select Data Setting

LDS	LD/f _{OUT} Output Signal
H	f _{OUT} signals
L	LD signals

Table 9. Charge Pump Current Setting

CS	Current Value
H	± 6.0 mA
L	± 1.5 mA



Power-Saving Mode (Intermittent Mode Control)

The Intermittent Mode Control circuit greatly reduces the PLL power consumption by shutting down various internal functions, as shown in Table 11, depending upon the settings of the power-save (PS) pins. (See the Electrical Characteristics chart for the specific value of current when in the power-saving mode.) In this mode, the phase detector output, Do, becomes high impedance and the lock detector output, LD, is as shown in Table 13. Setting the PS pin high releases the power-saving mode returning the selected PLL to normal operation.

The intermittent mode control circuit also ensures a smooth startup when the device returns to normal operation, at which time, the phase comparator output signal is unpredictable due to the unknown relationship between the comparison frequency (f_p) and the reference frequency (f_r). This can cause a major change in the comparator output, resulting in a VCO frequency jump and an increase in lock-up time.

To prevent a major VCO frequency jump, the Intermittent Mode Control circuit limits the magnitude of the error signal from the phase detector when it returns to normal operation.

Note: When power (V_{CC}) is first applied, the device must be in standby mode, PS = Low, for at least 1 μ s.

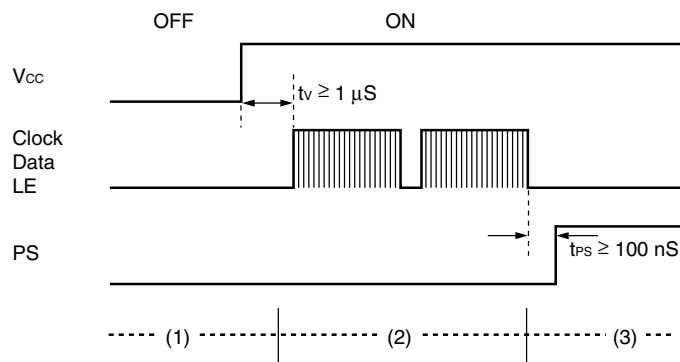
Table 10. Power-Save Pin Setting

PS Pins	Status
H	Normal mode
L	Power-saving mode

Table 11. Power-Save Internal Shutdown Logic

PS _{IF}	PS _{RF}	IF (TX)-PLL counters	RF (RX)-PLL counters	OSC input buffer
L	L	OFF	OFF	OFF
H	L	ON	OFF	ON
L	H	OFF	ON	ON
H	H	ON	ON	ON

Power-ON Timing



- (1) PS = L (power-saving mode) at Power ON
- (2) Set serial data 1 μ s later after power supply remains stable ($V_{CC} \geq 2.2\text{V}$).
- (3) Release power-saving mode (PS: L \rightarrow H) 100 ns later after setting serial data.

Dual PLL Frequency Synthesizers with On-Chip Prescalers

Serial Data Input Timing

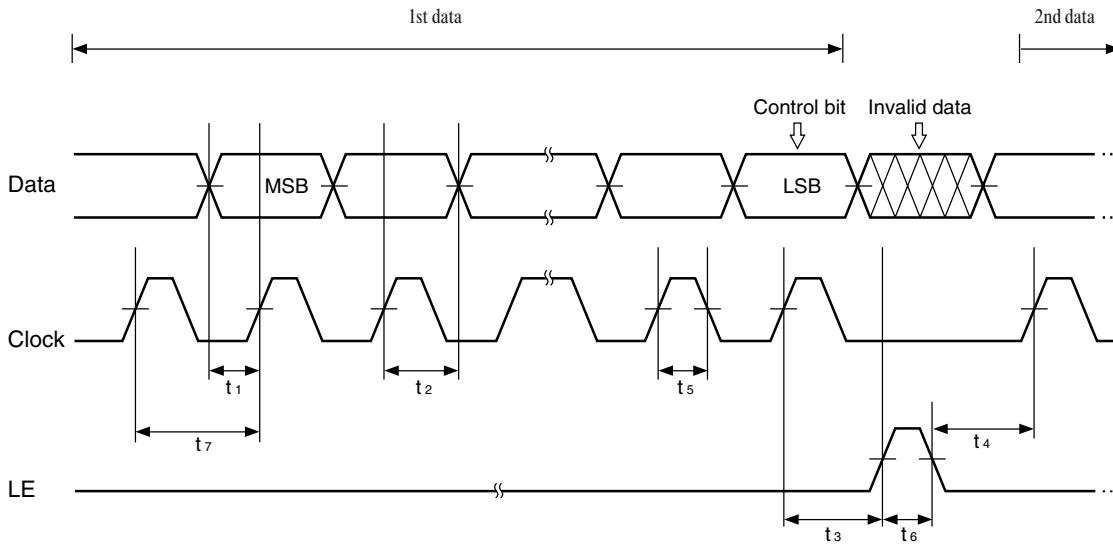


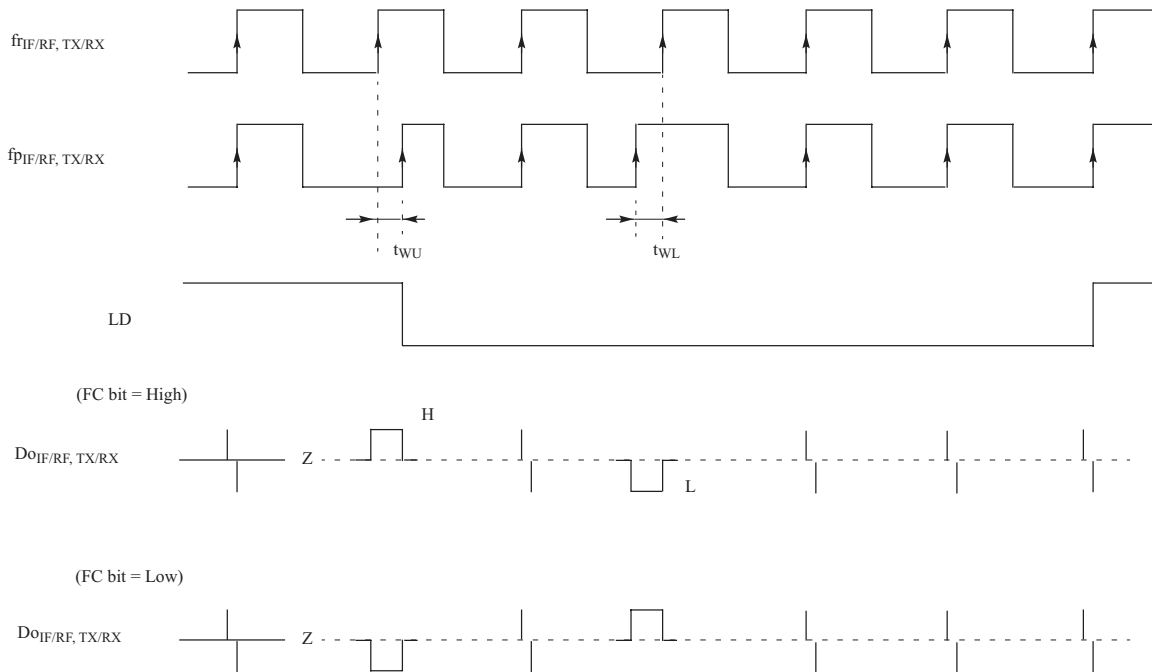
Table 12. Timing Parameters

Parameter	Min.	Typ.	Max.	Unit	Parameter	Min.	Typ.	Max.	Unit
t1	20	–	–	ns	t5	100	–	–	ns
t2	20	–	–	ns	t6	20	–	–	ns
t3	30	–	–	ns	t7	100	–	–	ns
t4	30	–	–	ns					

Notes: 1) On the rising edge of the clock, one bit of the data is transferred into the shift register.

2) LE should be "L" when the data is transferred into the shift register.

Phase Detector Output Waveform



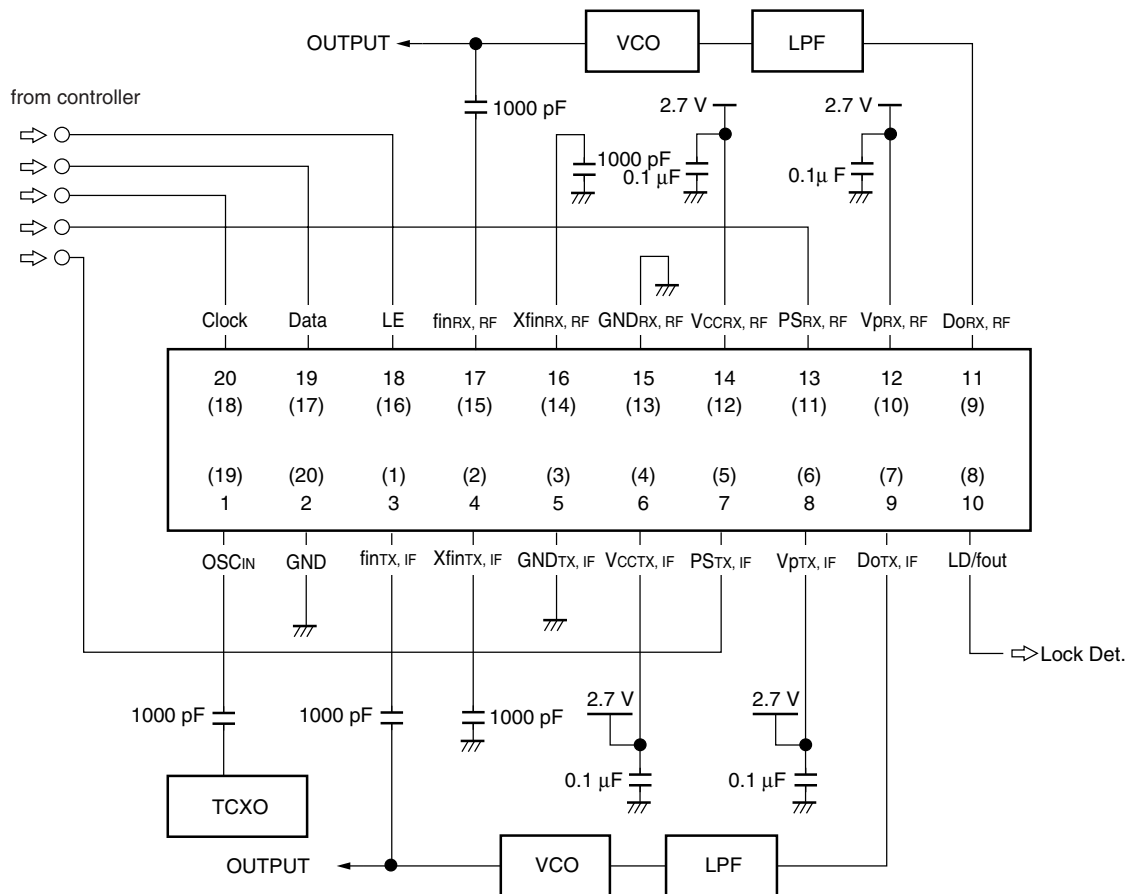
- Notes:
- 1) Phase error detection range: -2π to $+2\pi$
 - 2) Pulses on Do signal during locked state are output to prevent dead zone.
 - 3) LD output becomes low when phase is t_{WU} or more. LD output becomes high when phase error is t_{WL} or less and continues to be so for three cycles or more.
 - 4) t_{WU} and t_{WL} depend on OSC_{IN} input frequency.
 $t_{WU} \geq 2/f_{osc}$ (e. g. $t_{WU} \geq 156.3ns$, $f_{osc} = 12.8MHz$)
 $t_{WL} \leq 4/f_{osc}$ (e. g. $t_{WL} \leq 312.5ns$, $f_{osc} = 12.8MHz$)
 - 5) LD becomes high during the power-saving mode (PS = "L").

Table 13. LD Output Logic Table

IF/PLL1 Section	RF/PLL2 Section	LD Output
Locked state / Power-saving state	Locked state / Power-saving state	H
Locked state / Power-saving state	Unlocked state	L
Unlocked state	Locked state / Power-saving state	L
Unlocked state	Unlocked state	L

Dual PLL Frequency Synthesizers with On-Chip Prescalers

Application Example



Clock, Data, LE: Schmitt trigger circuit is provided (insert a pull-down or pull-up resistor to prevent oscillation when open-circuited in the input).

Note: ○ TSSOP-20
() BCC-20

Usage Precautions

$V_{CC_{RF/RX}}$ must equal $V_{CC_{IF/TX}}$. Even if either the RF/RX or IF/TX is not used, power must be supplied to both $V_{CC_{RF/RX}}$ and $V_{CC_{IF/TX}}$ to keep them equal. It is recommended that the unused PLL be controlled by the power-saving function.

To protect against damage by electrostatic discharge, note the following handling precautions:

- Store and transport devices in conductive containers.
- Use properly grounded workstations, tools, and equipment.
- Turn off power before inserting or removing this device into or from a socket.
- Protect leads with conductive sheet when transporting a board mounted device.

Ordering Information

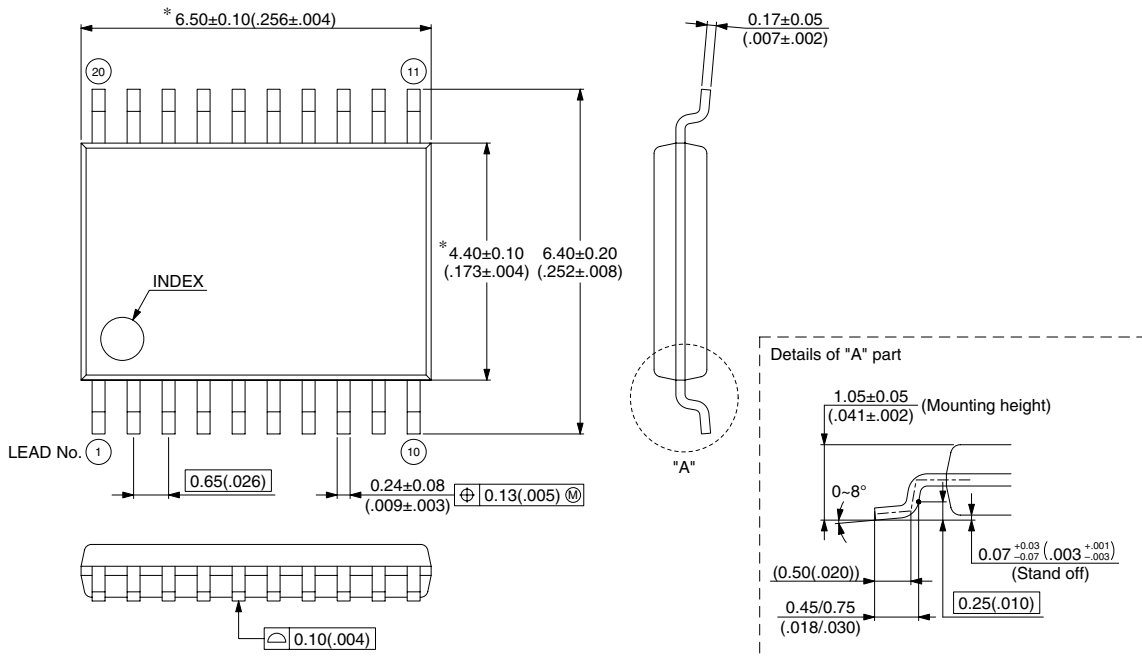
Part Number	Package
MB15F7xULPFT	20 pin, Plastic TSSOP (FPT-20P-M06)
MB15F7xULPVA	20 pin, Plastic BCC (LCC-20P-M05)

Dual PLL Frequency Synthesizers with On-Chip Prescalers

Package Dimensions

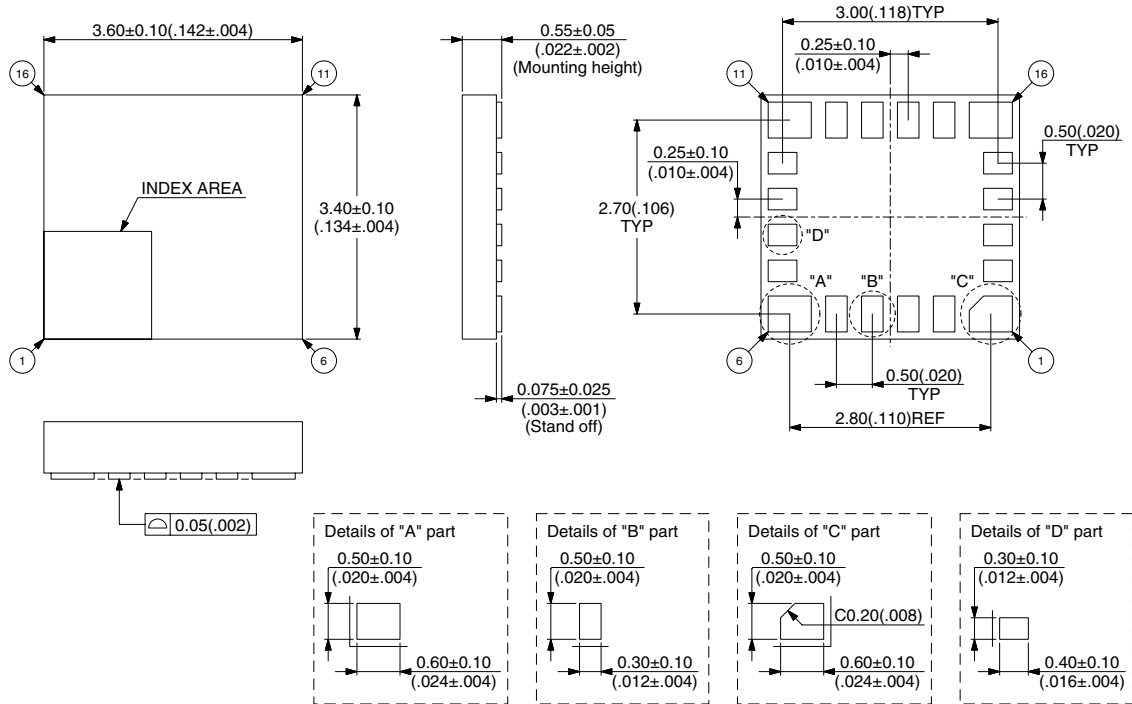
Note: 20-pin, Plastic SSOP (FPT-20P-M06)

* These dimensions do not include resin protrusion.



Package Dimensions

Note: 20-pad, Plastic BCC (LCC-20P-M05)



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