

ASSP

Dual Serial Input PLL Frequency Synthesizer(Small Package)

MB15F73UV

■ DESCRIPTION

The Fujitsu MB15F73UV is a serial input Phase Locked Loop (PLL) frequency synthesizer with a 2250MHz and a 600MHz prescalers. A 64/65 or a 128/129 for the 2250MHz prescaler, and a 8/9 or a 16/17 for the 600MHz prescaler can be selected for the prescaler that enables pulse swallow operation.

The latest BiCMOS process is used, as a result a supply current is typically 3.2mA typ. at 2.7V. The supply voltage range is from 2.4V to 3.6V. A refined charge pump supplies well-balanced output current with 1.5mA and 6mA selectable by serial data. The data format and the function as fast locking are same as the previous one MB15F73UL.

The new package(BCC18) decreases a mount area of MB15F73UV about 50% comparing with the former BCC20(for dual PLL, MB15F73UL).

MB15F73UV is ideally suited for wireless mobile communications, such as CDMA.

■ FEATURES

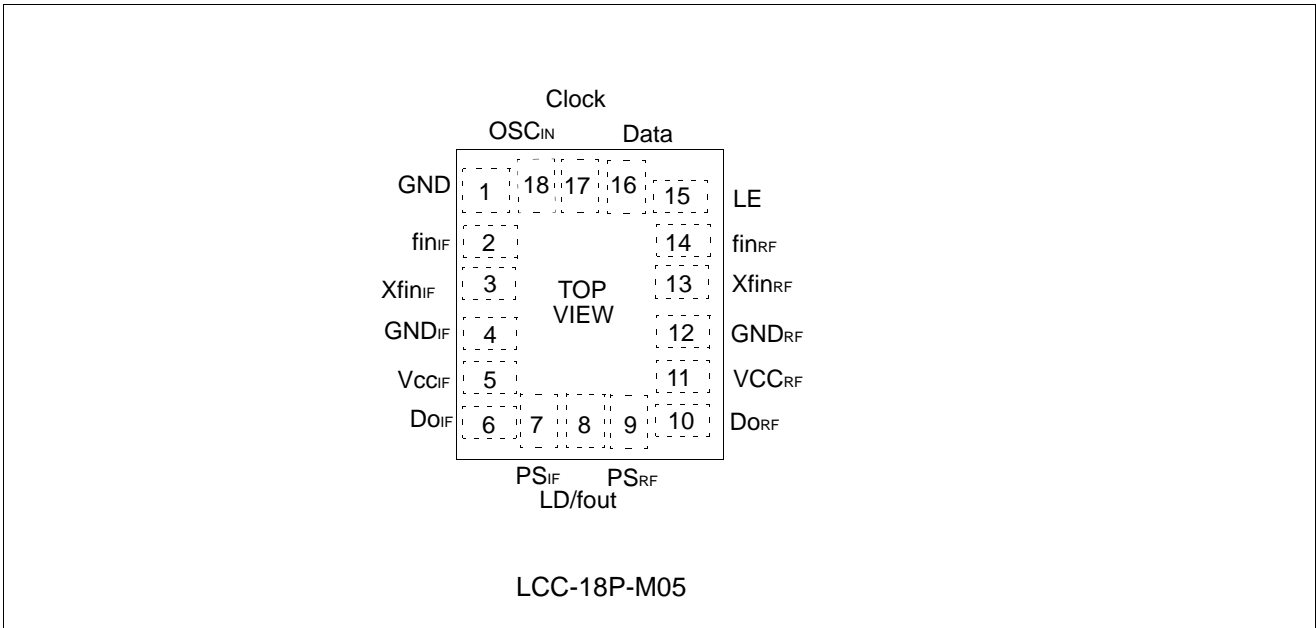
- Very small package: BCC18 (2.4*2.7*0.5mm)
- High frequency operation: RF synthesizer : 2250MHz max
IF synthesizer : 600MHz max
- Low power supply voltage: $V_{CC} = 2.4$ to 3.6 V
- Ultra Low power supply current : $I_{CC} = 3.2$ mA typ. ($V_{CC} = 2.7V$, $T_a = 25^\circ C$, $SW=0$ in RF, IF locking state)
- Direct power saving function : Power supply current in power saving mode
Typ. $0.1 \mu A$ ($V_{CC}=2.7V$, $T_a=25^\circ C$), Max. $10 \mu A$ ($V_{CC}=2.7V$)
- Dual modulus prescaler : 2250MHz prescaler(64/65 or 128/129) / 600MHz prescaler(8/9 or 16/17)
- Serial input 14-bit programmable reference divider: $R = 3$ to 16,383
- Serial input programmable divider consisting of:
 - Binary 7-bit swallow counter: 0 to 127
 - Binary 11-bit programmable counter: 3 to 2,047
- On-chip phase comparator for fast lock and low noise
- On-chip phase control for phase comparator
- Operating temperature: $T_a = -40$ to $85^\circ C$
- Sireal data format compatible with MB15F73UL

18-pad, Plastic BCC



(LCC-18P-M05)

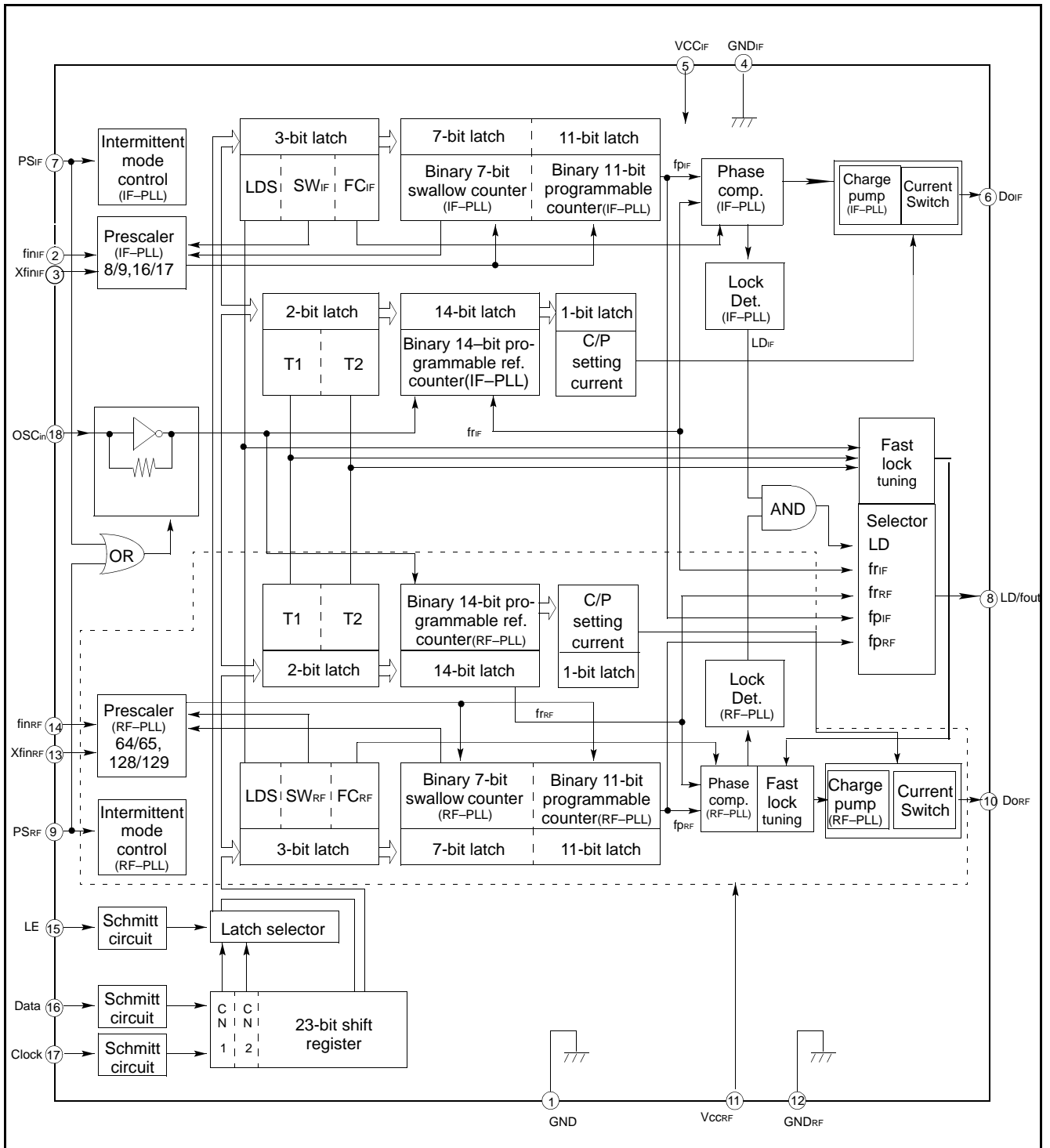
■ PIN ASSIGNMENT



■ **PIN DESCRIPTIONS**

| Pin No. | Pin name | I/O | Descriptions |
|---------|--------------------|-----|--|
| 1 | GND | - | Ground for OSC input buffer and the shift register circuit. |
| 2 | fin _{IF} | I | Prescaler input pin for the IF-PLL section. Connection to an external VCO should be AC coupling. |
| 3 | Xfin _{IF} | I | Prescaler complimentary input for the IF-PLL section. This pin should be grounded via a capacitor. |
| 4 | GND _{IF} | - | Ground for the IF-PLL section. |
| 5 | VCC _{IF} | - | Power supply voltage input pin for the IF-PLL section(except for the charge pump circuit), the shift register and the oscillator input buffer. When power is OFF, latched data of IF-PLL is lost. |
| 6 | DO _{IF} | O | Charge pump output for the IF-PLL section. Phase characteristics of the phase detector can be reversed by FC-bit. |
| 7 | PS _{IF} | I | Power saving mode control for the IF-PLL section. This pin must be set at "L" Power-ON. (Open is prohibited.) PS _{IF} = "H" ; Normal mode PS _{IF} = "L" ; Power saving mode |
| 8 | LD/fout | O | Lock detect signal output(LD)/ phase comparator monitoring outut (fout). The output signal is selected by a LDS bit in a serial data. LDS bit = "1" ; outputs fout signal LDS bit = "0" ; outputs LD signal |
| 9 | PS _{RF} | I | Power saving mode control for the RF-PLL section. This pin must be set at "L" Power-ON. (Open is prohibited.) PS _{RF} = "H" ; Normal mode PS _{RF} = "L" ; Power saving mode |
| 10 | DO _{RF} | O | Charge pump output for the RF-PLL section. Phase characteristics of the phase detector can be reversed by FC-bit. |
| 11 | VCC _{RF} | - | Power supply voltage input pin for the RF-PLL section(except for the charge pump circuit). |
| 12 | GND _{RF} | - | Ground for the RF-PLL section. |
| 13 | Xfin _{RF} | I | Prescaler complimentary input for the RF-PLL section. This pin should be grounded via a capacitor. |
| 14 | fin _{RF} | I | Prescaler input pin for the RF-PLL. Connction to an external VCO should be AC coupling. |
| 15 | LE | I | Load enable signal input (with the schmitt trigger circuit.) When LE is set "H", data in the shift register is transferred to the corresponding latch according to the control bit in a serial data. |
| 16 | Data | I | Serial data input (with the schmitt trigger circuit.) A data is transferred to the corresponding latch (IF-ref counter, IF-prog. counter, RF-ref. counter, RF-prog. counter) according to the control bit in a serial data. |
| 17 | Clock | I | Clock input for the 23-bit shift register (with the schmitt trigger circuit.) One bit data is shifted into the shift register on a rising edge of the clock. |
| 18 | OSC _{IN} | I | The programmable reference divider input. TCXO should be connected with a AC coupling capacitor. |

■ BLOCK DIAGRAM



■ **ABSOLUTE MAXIMUM RATINGS**

| Parameter | Symbol | Rating | Unit | Remark |
|----------------------|-----------|------------------------|------|---------|
| Power supply voltage | V_{CC} | -0.5 to +4.0 | V | |
| Input voltage | V_I | -0.5 to $V_{CC} + 0.5$ | V | |
| Output voltage | V_O | GND to V_{CC} | V | LD/fout |
| | V_{DO} | GND to V_{CC} | V | Do |
| Storage temperature | T_{stg} | -55 to +125 | °C | |

Note: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

■ **RECOMMENDED OPERATING CONDITIONS**

| Parameter | Symbol | Value | | | Unit | Remark |
|-----------------------|----------|-------|------|----------|------|-----------------------|
| | | Min. | Typ. | Max. | | |
| Power supply voltage | V_{CC} | 2.4 | 2.7 | 3.6 | V | $V_{CCRF} = V_{CCIF}$ |
| Input voltage | V_I | GND | - | V_{CC} | V | |
| Operating temperature | T_a | -40 | - | +85 | °C | |

Handling Precautions

- (1) V_{CCRF} and V_{CCIF} must supply equal voltage.
Even if either RF-PLL or IF-PLL is not used, power must be supplied to both V_{CCRF} and V_{CCIF} to keep them equal. It is recommended that the non-use PLL is controlled by power saving function.
- (2) To protect against damage by electrostatic discharge, note the following handling precautions:
 - Store and transport devices in conductive containers.
 - Use properly grounded workstations, tools, and equipment.
 - Turn off power before inserting or removing this device into or from a socket.
 - Protect leads with conductive sheet, when transporting a board mounted device.

■ ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.4 to 3.6 V, T_a = -40 to +85°C)

| Parameter | | Symbol | Condition | Value | | | Unit |
|-------------------------------|--------------------------------------|--------------------|--|------------------------------|------------------|------------------------------|------|
| | | | | Min. | Typ. | Max. | |
| Power supply current*1 | | I _{CCIF} | f _{inIF} =480MHz V _{CCIF} =2.7V | 0.8 | 1.2 | 1.7 | mA |
| | | I _{CCRF} | f _{inRF} =2250MHz V _{CCRF} =2.7V | 1.3 | 2.0 | 2.8 | mA |
| Power saving current*9 | | I _{PSIF} | PS _{IF} =PS _{RF} = "L" | - | 0.1 ² | 10 | μA |
| | | I _{PSRF} | PS _{IF} =PS _{RF} = "L" | - | 0.1 ² | 10 | μA |
| Operating frequency | f _{inIF} *3 | f _{inIF} | IF PLL | 50 | - | 600 | MHz |
| | f _{inRF} *3 | f _{inRF} | RF PLL | 200 | - | 2250 | MHz |
| | OSC _{IN} | f _{osc} | - | 3 | - | 40 | MHz |
| Input sensitivity | f _{inIF} | Pf _{inIF} | IF PLL, 50 Ω system | -15 | - | +2 | dBm |
| | f _{inRF} | Pf _{inRF} | RF PLL, 50 Ω system | -15 | - | +2 | dBm |
| | OSC _{IN} | V _{OSC} | - | 0.5 | - | 1.5 | Vp-p |
| "H" level Input voltage | Data, Clock, LE | V _{IH} | Schmitt trigger input | V _{CC} × 0.7+0.4 | - | - | V |
| "L" level Input voltage | | V _{IL} | Schmitt trigger input | - | - | V _{CC} × 0.3-0.4 | |
| "H" level Input voltage | PS | V _{IH} | - | V _{CC} × 0.7 | - | - | V |
| "L" level Input voltage | | V _{IL} | - | - | - | V _{CC} × 0.3 | |
| "H" level Input current | Data, Clock, LE, PS | I _{IH} *4 | - | -1.0 | - | +1.0 | μA |
| "L" level Input current | | I _{IL} *4 | - | -1.0 | - | +1.0 | |
| "H" level output voltage | LD/fout | V _{OH} | V _{CC} =2.7V, I _{OH} =-1mA | V _{CC} - 0.4 | - | - | V |
| "L" level output voltage | | V _{OL} | V _{CC} =2.7V, I _{OL} =1mA | - | - | 0.4 | |
| "H" level output voltage | DO _{IF} DO _{RF} | V _{DOH} | V _{CC} =2.7V, I _{DOH} =-0.5mA | V _{CC} - 0.4 | - | - | V |
| "L" level output voltage | | V _{DOL} | V _{CC} =2.7V, I _{DOL} =0.5mA | - | - | 0.4 | |
| High impedance cutoff current | DO _{IF} DO _{RF} | I _{OFF} | V _{CC} =2.7V, V _{OFF} =0.5V to V _p -0.5V | - | - | 2.5 | nA |
| "H" level Output current | LD/fout | I _{OH} *4 | V _{CC} = 2.7V | - | - | -1.0 | mA |
| "L" level Output current | | I _{DOL} | V _{CC} = 2.7V | 1.0 | - | - | |

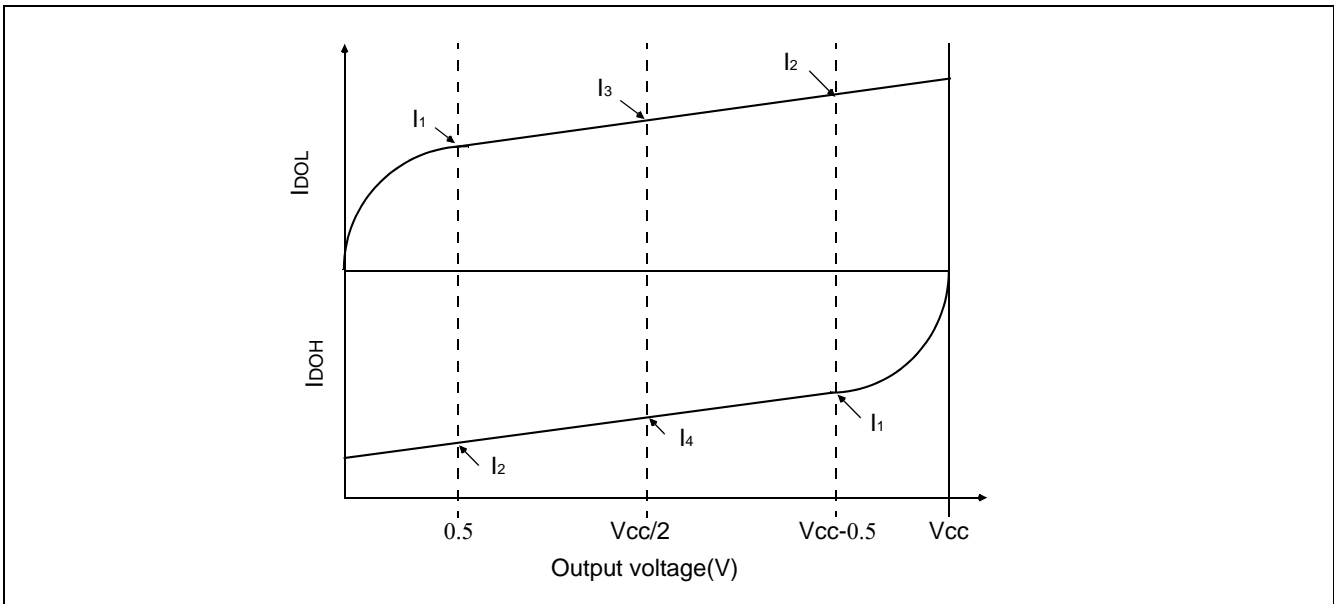
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(V_{CC} = 2.4 to 3.6 V, T_a = -40 to +85°C)

| Parameter | Symbol | Condition | Value | | | Unit | | |
|--------------------------|--|---------------------------------|---|--------------|------|------|------|----|
| | | | Min. | Typ. | Max. | | | |
| "H" level Output current | D _{OTX} ^{*8} D _{ORX} | I _{DOH} ^{*4} | V _{CC} =2.7 V V _{DOH} =V _{CC} /2 T _a = 25°C | CS bit = "1" | -8.2 | -6.0 | -4.1 | mA |
| | | | CS bit = "0" | -2.2 | -1.5 | -0.8 | | |
| "L" level Output current | | I _{DOL} | V _{CC} =2.7 V V _{DOL} =V _{CC} /2 T _a = 25°C | CS bit = "1" | 4.1 | 6.0 | 8.2 | |
| | | | | CS bit = "0" | 0.8 | 1.5 | 2.2 | |
| Charge pump current rate | I _{DOL} /I _{DOH} | I _{DOMT} ^{*5} | V _{DO} =V _{CC} /2 | - | 3 | - | % | |
| | vs V _{DO} | I _{DOVD} ^{*6} | 0.5V ≤ V _{DO} ≤ V _{CC} -0.5V | - | 10 | - | % | |
| | vs T _a | I _{DOTA} ^{*7} | -40°C ≤ T _a ≤ 85 °C, V _{DO} =V _{CC} /2 | - | 5 | - | % | |

- *1: Conditions; fosc=12.8MHz, T_a = 25°C, SW="L" in locking state.
- *2: V_{CC}=2.7V, fosc=12.8MHz, T_a = 25°C, in power saving mode.
- *3: AC coupling. 1000pF capacitor is connected under the condition of min. operating frequency.
- *4: The symbol "-"(minus) means direction of current flow.
- *5: V_{CC}=2.7V, T_a=25°C $(|I_3| - |I_4|) / [(|I_3| + |I_4|) / 2] \times 100(\%)$
- *6: V_{CC}=2.7V, T_a=25°C $[(|I_2| - |I_1|) / 2] / [(|I_1| + |I_2|) / 2] \times 100(\%)$ (Applied to each I_{DOL}, I_{DOH})
- *7: V_{CC}=2.7V, $(|I_{DO(85C)}| - |I_{DO(-40C)}|) / 2 / [(|I_{DO(85C)}| + |I_{DO(-40C)}|) / 2] \times 100(\%)$ (Applied to each I_{DOL}, I_{DOH})
- *8: When Charge pump current is measured, set LDS="0", T1="0" and T2="1".
- *9: PS_{IF}=PS_{RF}=GND (V_{IL}=GND and V_{IH}=V_{CC} for Clock, Data, LE)



■ FUNCTIONAL DESCRIPTIONS

The divide ratio can be calculated using the following equation:

$$f_{VCO} = \{(P \times N) + A\} \times f_{osc} \div R$$

- f_{VCO}: Output frequency of external voltage controlled oscillator (VCO)
- P: Preset divide ratio of dual modulus prescaler (8 or 16 for IF-PLL, 64 or 128 for RF-PLL)
- N: Preset divide ratio of binary 11-bit programmable counter (3 to 2,047)
- A: Preset divide ratio of binary 7-bit swallow counter (0 ≤ A ≤ 127, condition; A < N)
- f_{osc}: Reference oscillation frequency
- R: Preset divide ratio of binary 14-bit programmable reference counter (3 to 16,383)

Serial Data Input

Serial data is entered using three pins, Data pin, Clock pin, and LE pin. Programmable dividers of IF/RF-PLL sections, programmable reference dividers of IF/RF-PLL sections are controlled individually.

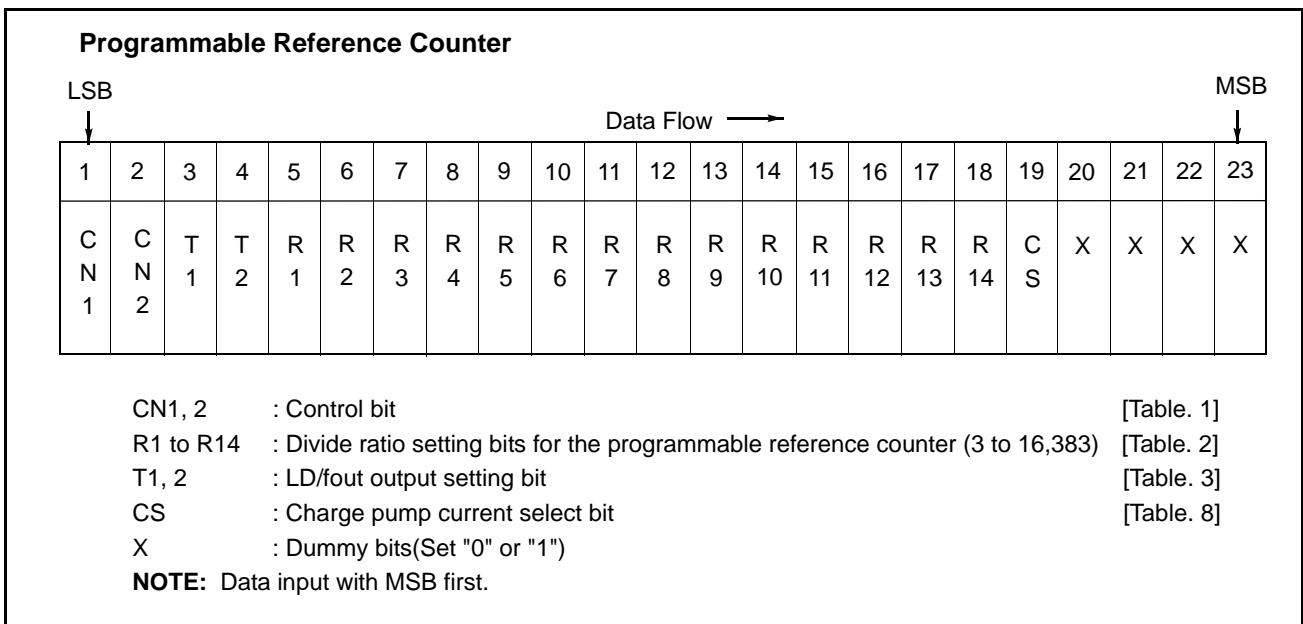
Serial data of binary data is entered through Data pin.

On a rising edge of clock, one bit of serial data is transferred into the shift register. On a rising edge of load enable signal, the data stored in the shift register is transferred to one of latch of them depending upon the control bit data setting.

Table1. Control Bit

| Control bit | | Destination of serial data |
|-------------|-----|---|
| CN1 | CN2 | |
| 0 | 0 | The programmable reference counter for the IF-PLL. |
| 1 | 0 | The programmable reference counter for the RF-PLL. |
| 0 | 1 | The programmable counter and the swallow counter for the IF-PLL |
| 1 | 1 | The programmable counter and the swallow counter for the RF-PLL |

Shift Register Configuration



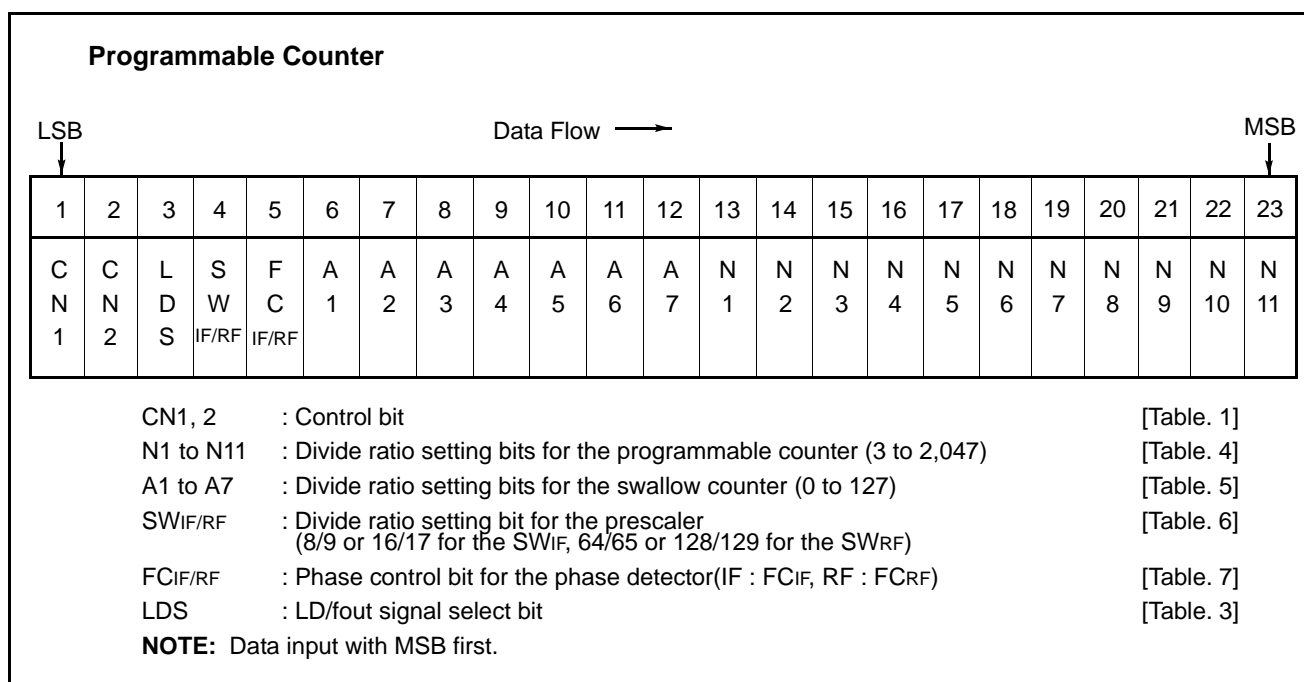


Table2. Binary 14-bit Programmable Reference Counter Data Setting

| Divide ratio (R) | R 14 | R 13 | R 12 | R 11 | R 10 | R 9 | R 8 | R 7 | R 6 | R 5 | R 4 | R 3 | R 2 | R 1 |
|------------------|------|------|------|------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 4 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| . | . | . | . | . | . | . | . | . | . | . | . | . | . | . |
| 16383 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Note: • Divide ratio less than 3 is prohibited.

Table.3 LD/fout output Selectable Bit Setting

| LD/fout pin state | | LDS | T1 | T2 |
|-------------------|------|-----|----|----|
| LD output | | 0 | 0 | 0 |
| | | 0 | 1 | 0 |
| | | 0 | 1 | 1 |
| fout output | frIF | 1 | 0 | 0 |
| | frRF | 1 | 1 | 0 |
| | fpIF | 1 | 0 | 1 |
| | fpRF | 1 | 1 | 1 |

Table.4 Binary 11-bit Programmable Counter Data Setting

| Divide ratio (N) | N 11 | N 10 | N 9 | N 8 | N 7 | N 6 | N 5 | N 4 | N 3 | N 2 | N 1 |
|------------------|------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 4 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| . | . | . | . | . | . | . | . | . | . | . | . |
| 2047 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Note: • Divide ratio less than 3 is prohibited.

Table.5 Binary 7-bit Swallow Counter Data Setting

| Divide ratio (N) | A 7 | A 6 | A 5 | A 4 | A 3 | A 2 | A 1 |
|------------------|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| . | . | . | . | . | . | . | . |
| 127 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Note: • Divide ratio (A) range = 0 to 127

Table. 6 Prescaler Data Setting

| | | SW = "1" | SW = "0" |
|------------------------|--------|----------|----------|
| Prescaler divide ratio | IF-PLL | 8/9 | 16/17 |
| | RF-PLL | 64/65 | 128/129 |

Table. 7 Phase Comparator Phase Switching Data Setting

| | FC _{IF,RF} = 1 | FC _{IF,RF} = 0 |
|--------------|-------------------------|-------------------------|
| | Do _{IF,RF} | |
| fr > fp | H | L |
| fr = fp | Z | Z |
| fr < fp | L | H |
| VCO polarity | 1 | 2 |

Note: • Z = High-impedance
• Depending upon the VCO and LPF polarity, FC bit should be set.

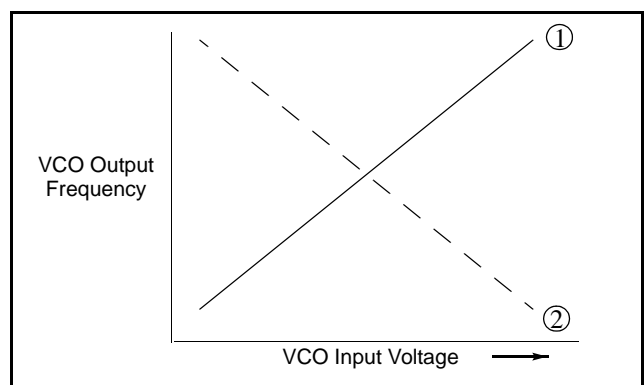


Table. 8 Charge Pump Current Setting

| CS | Current value |
|-----------|----------------------|
| 1 | ± 6.0 mA |
| 0 | ± 1.5 mA |

4. Power Saving Mode (Intermittent Mode Control Circuit)

Table 9. PS Pin Setting

| PS pin | Status |
|---------------|-------------------|
| H | Normal mode |
| L | Power saving mode |

The intermittent mode control circuit reduces the PLL power consumption.

By setting the PS pin low, the device enters into the power saving mode, reducing the current consumption. See the Electrical Characteristics chart for the specific value.

The phase detector output, Do, becomes high impedance.

For the single PLL, the lock detector, LD, remains high, indicating a locked condition.

For the dual PLL, the lock detector, LD, is as shown in the LD Output Logic table.

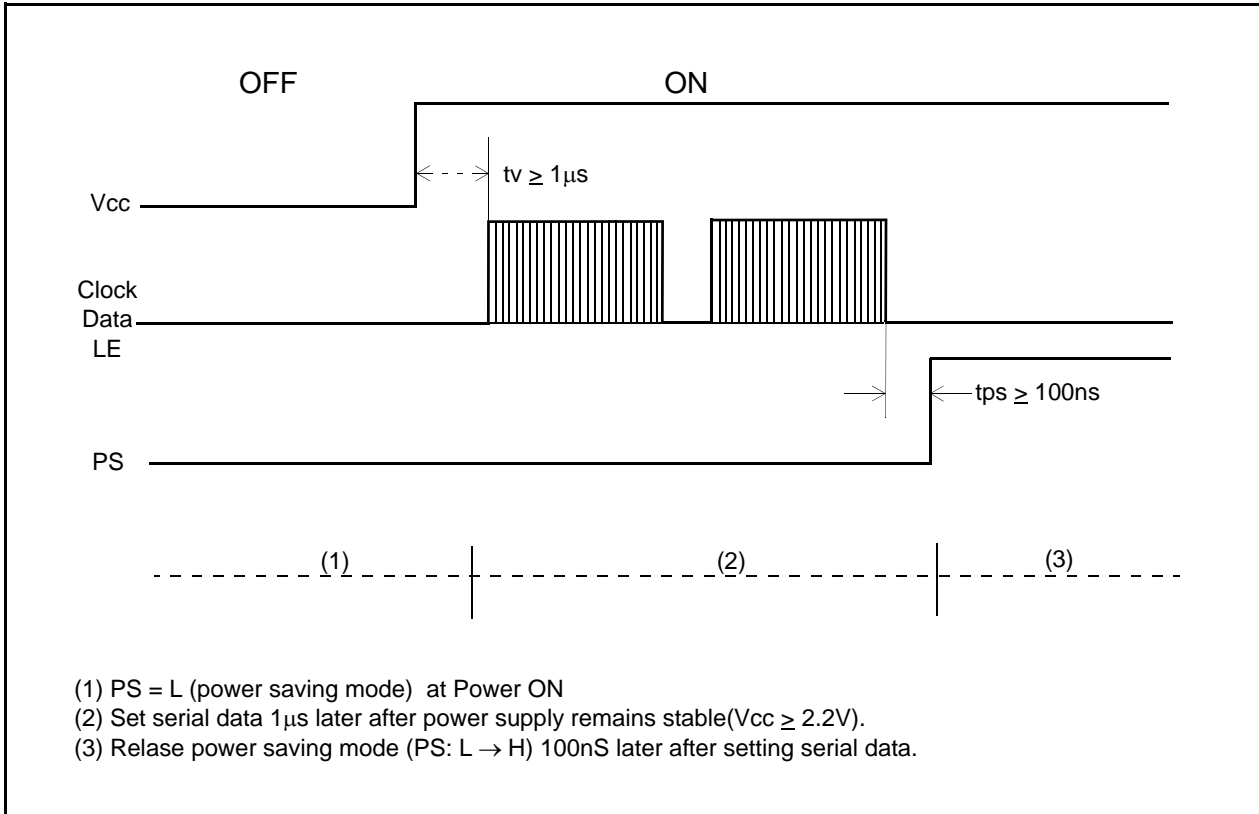
Setting the PS pin high, releases the power saving mode, and the device works normally.

The intermittent mode control circuit also ensures a smooth startup when the device returns to normal operation. When the PLL is returned to normal operation, the phase comparator output signal is unpredictable. This is because of the unknown relationship between the comparison frequency (f_p) and the reference frequency (f_r) which can cause a major change in the comparator output, resulting in a VCO frequency jump and an increase in lockup time.

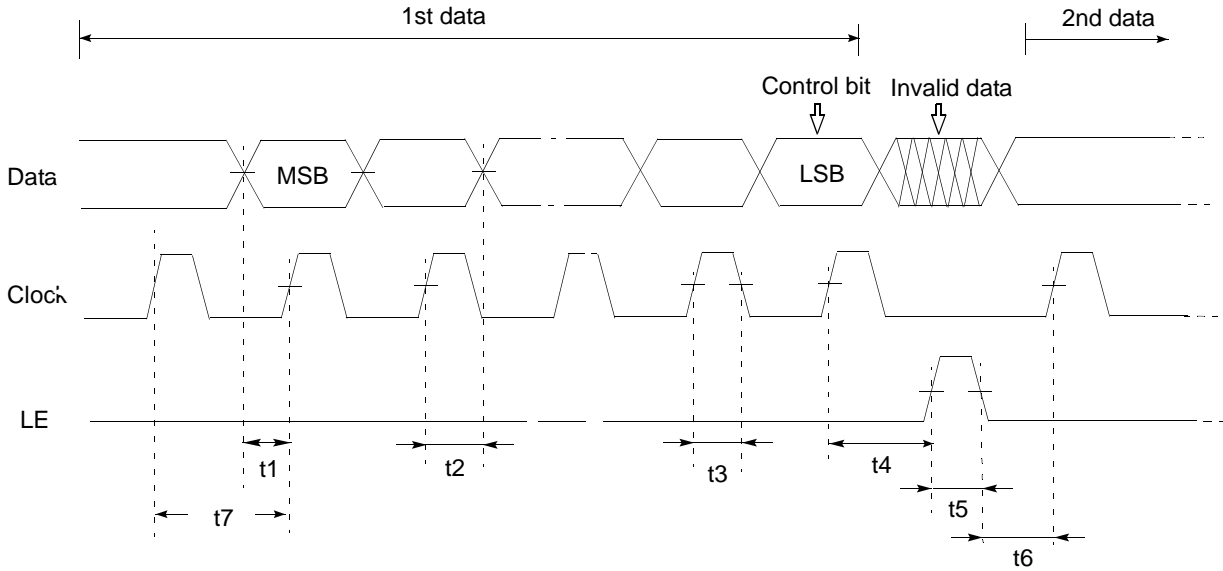
To prevent a major VCO frequency jump, the intermittent mode control circuit limits the magnitude of the error signal from the phase detector when it returns to normal operation.

Note: When power (V_{cc}) is first applied, the device must be in standby mode.

Note: • PS pin must be set at “L” for Power ON.



■ SERIAL DATA INPUT TIMING

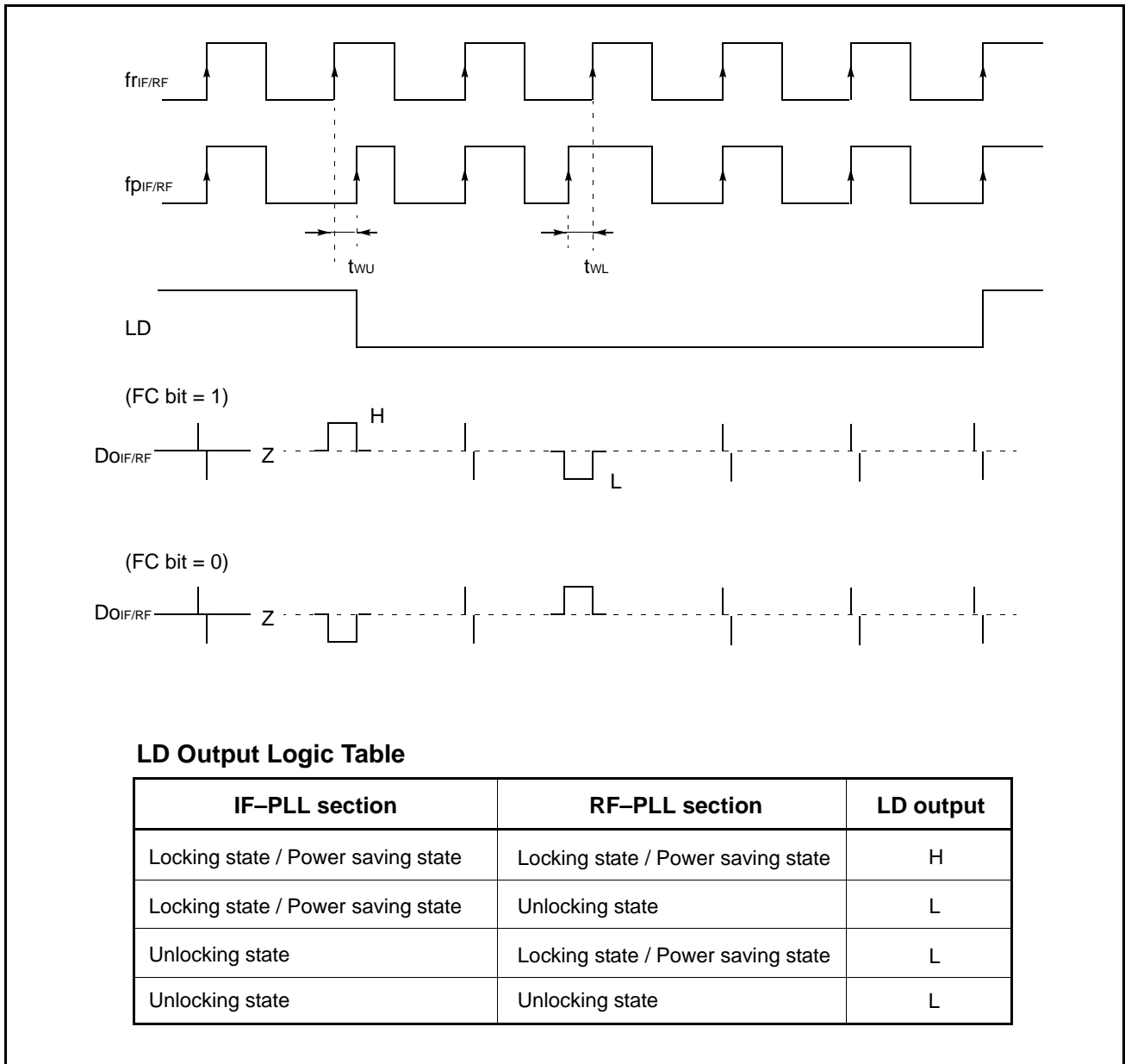


On the rising edge of the clock, one bit of data is transferred into the shift register.

| Parameter | Min. | Typ. | Max. | Unit | Parameter | Min. | Typ. | Max. | Unit |
|-----------|------|------|------|------|-----------|------|------|------|------|
| t1 | 20 | – | – | ns | t5 | 100 | – | – | ns |
| t2 | 20 | – | – | ns | t6 | 20 | – | – | ns |
| t3 | 30 | – | – | ns | t7 | 100 | – | – | ns |
| t4 | 30 | – | – | ns | | | | | |

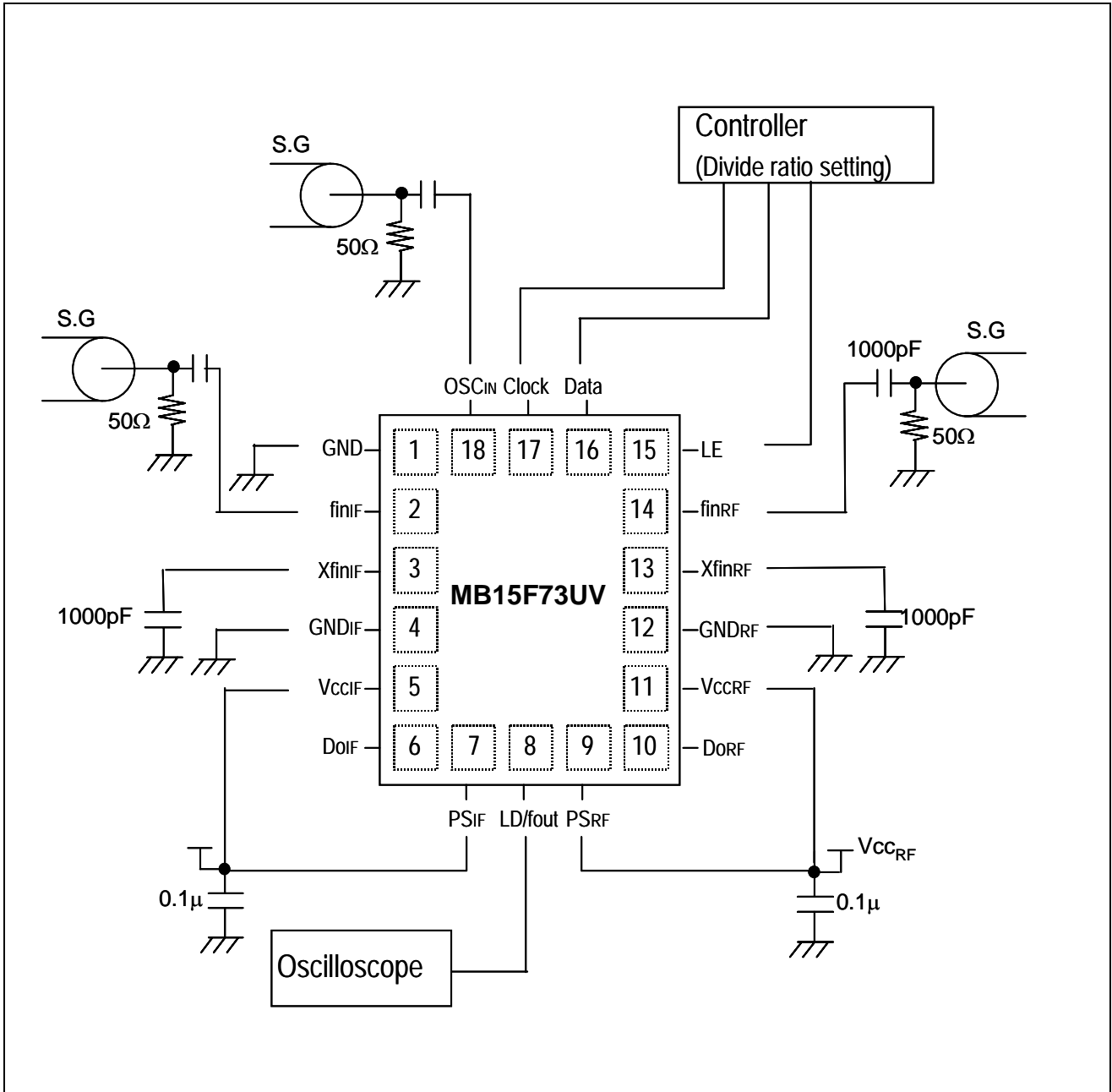
Note: LE should be "L" when the data is transferred into the shift register.

■ PHASE DETECTOR OUTPUT WAVEFORM

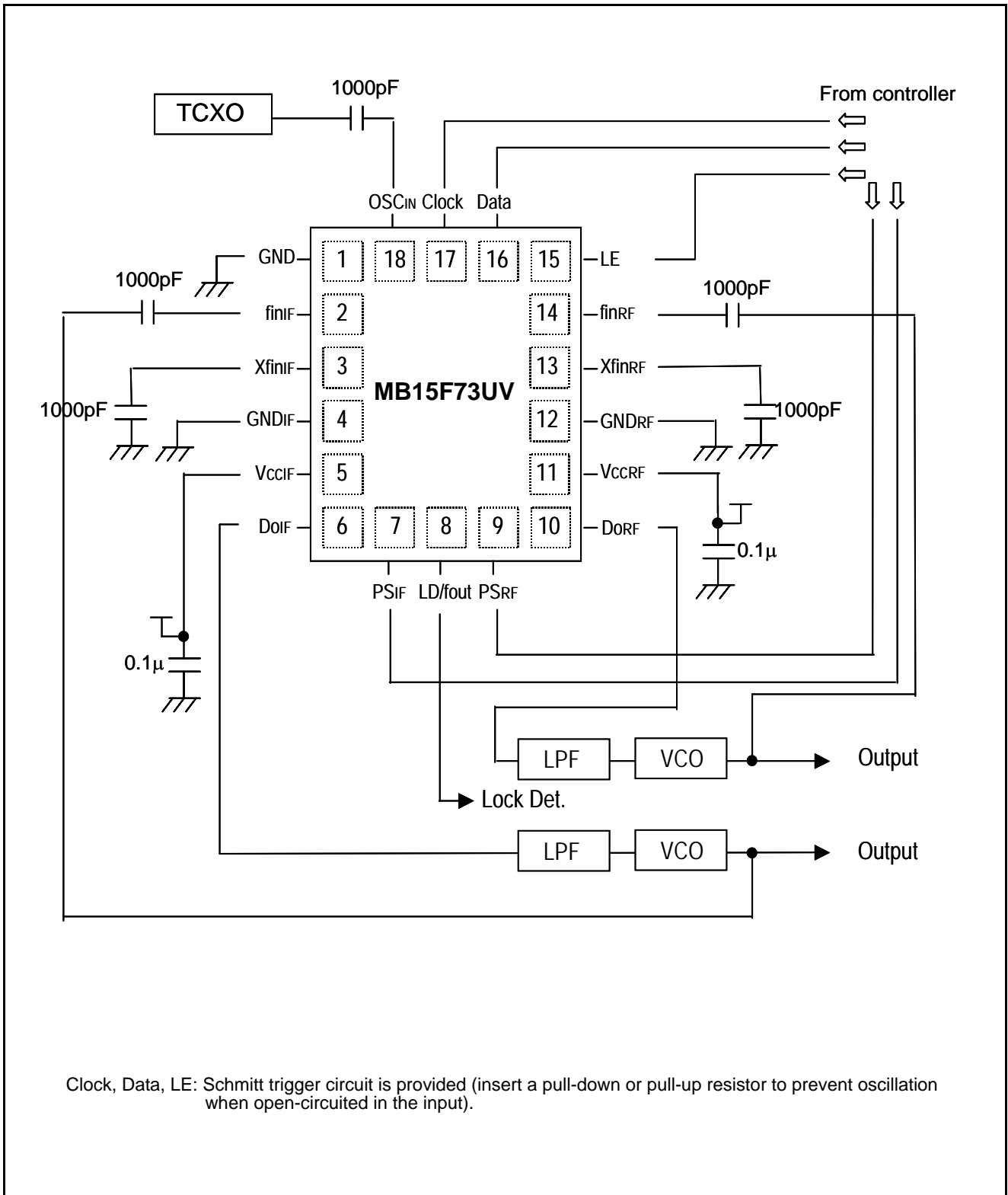


- Note:
- Phase error detection range = -2π to $+2\pi$
 - Pulses on D_{OIF/RF} signals are output to prevent dead zone.
 - LD output becomes low when phase error is t_{WU} or more.
 - LD output becomes high when phase error is t_{WL} or less and continues to be so for three cycles or more.
 - t_{WU} and t_{WL} depend on OSCin input frequency as follows.
 t_{WU} ≥ 2/fosc: i.e. t_{WU} ≥ 156.3ns when foscin = 12.8 MHz
 t_{WL} ≤ 4/fosc: i.e. t_{WL} ≤ 312.5ns when foscin = 12.8 MHz

■ **TEST CIRCUIT** (for Measuring Input Sensitivity f_{in}/OSC_{in})



■ APPLICATION EXAMPLE



■ PACKAGE DIMENSION

