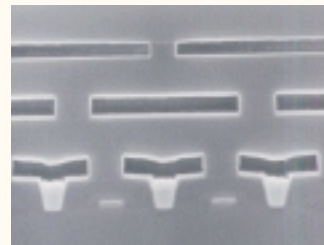
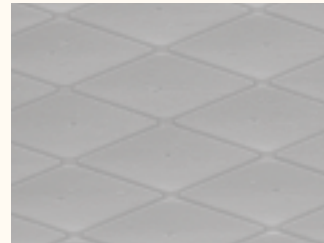


# LCOS Backplane Process

## ► Features

- 0.65 $\mu$ m/0.5 $\mu$ m/0.35 $\mu$ m FEOL
  - Supply Voltage: 3.3V/5.0V
  - Option: High voltage (13V/25V)  
Diffusion Resistor  
Bulk-Poly capacitor
- 0.35 $\mu$ m BEOL
  - CMP planarization for dielectric layers
  - Perfect planarization between Pixels
  - Tungsten plugs for via
  - Stack Via available
  - Optimized anti-reflection layers
  - High reflectivity in 400-700nm optical spectrum
- Future Process Technology
  - 0.25 $\mu$ m FEOL/BEOL
  - Supply Voltage: 2.5V/3.3V
  - Option: Diffusion Resistor  
Poly-Poly capacitor



# CMOS Image Sensor Process

## ► Features

- 0.35 $\mu$ m Process
  - Supply Voltage: 3.3V/5.0V
  - Sensor Type: Photodiode
  - Low Dark current (<0.1nA/cm<sup>2</sup>)
  - Resolution: Up to SXGA
- 0.25 $\mu$ m process is under development  
Target: 2Q/2002
- 0.18 $\mu$ m process is in the planning stage



1/4 inch VGA (350k pixels)

# High Voltage Process

Features			
	0.65μm	0.50μm	0.35μm
Process	1P2M	1P3M	2P4M
Logic	5.0V	3.3V	3.3V
High Voltage	25V/35V	13V	15V/20V/30V
Mask Data			
Acceptance	Now	Now	2002.1Q
Production	Now/2001.4Q	Now	2002.2Q

Options		
	0.65/0.5μm	0.35μm
Capacitor	Bulk-Poly	Bulk-Poly/ Poly-Poly
Resistor	Diffusion Resistor	Diffusion/Poly Resistor

