

# FRAM Low-Voltage Sensing Technology

FUJITSU recently invented a FRAM-sensing method that can effectively apply voltage to the cell capacitor even under low-voltage power supply conditions, essentially by reading the bit-line potential in the proximity of the GND potential. This article introduces a FRAM memory voltage reduction technology that adopts this new sensing method.

## Introduction

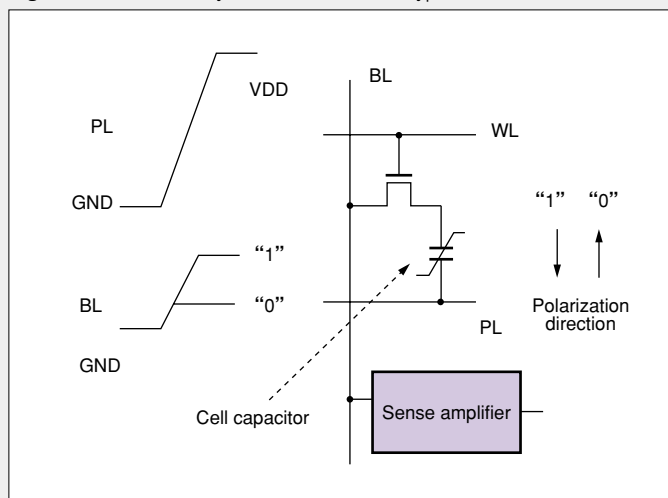
FRAM is a non-volatile memory device that adopts ferroelectric film in the memory cell. Using "remnant polarization," a property of ferroelectric film that makes it possible to maintain polarization without adding an electric field, the memory data can be stored as the "0" and "1" directions of polarization. FRAM is as nonvolatile as ROM, and can read/write at speed as high as SRAM. And since FRAM consumes little power, it can be mounted on non-contact type Smart cards. The application of the Smart card—a combination of an IC card mounting

microcontroller, storage circuit, and RF circuit—is expected to expand into markets such as electronic money, medical cards, amusement cards, and so on.

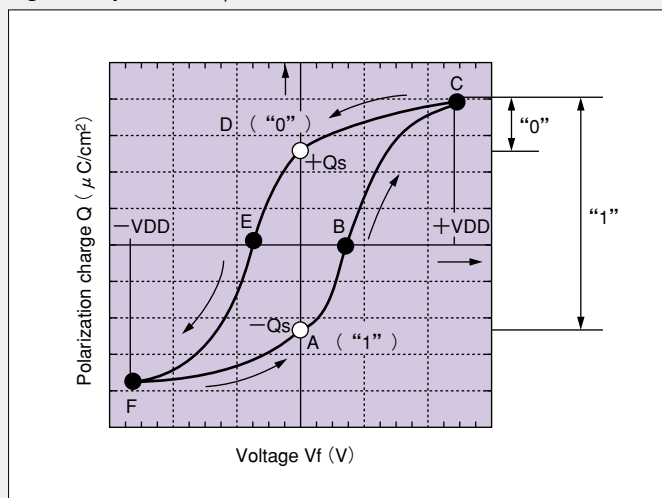
FRAM has good compatibility with the CMOS process, and can thus be consolidated with logic circuits and RF circuits on the LSI chips to be used in Smart cards. As voltages are steadily reduced in logic circuit progresses in the future, this capability is expected to bolster the demand for low-voltage-operation FRAM circuits.

This article introduces a FRAM memory voltage reduction technology that adopts a new sensing method.

**Figure 1** FRAM Memory Cell Structure (1T1C-Type)



**Figure 2** Hysteresis Loop



## FRAM Operation Principle

**Fig. 1** shows the FRAM memory cell configuration in a 1T1C-type cell (one ferroelectric capacitor and one transistor). When voltage is applied between the bit line (BL) and the plate line (PL) with the word line (WL) selected, the voltage flows to the cell capacitor for the writing of specified data (polarization direction). The BL=0V and PL=VDD settings are used to write in a “0,” and the BL=VDD and PL=0V settings are used to write in a “1.”

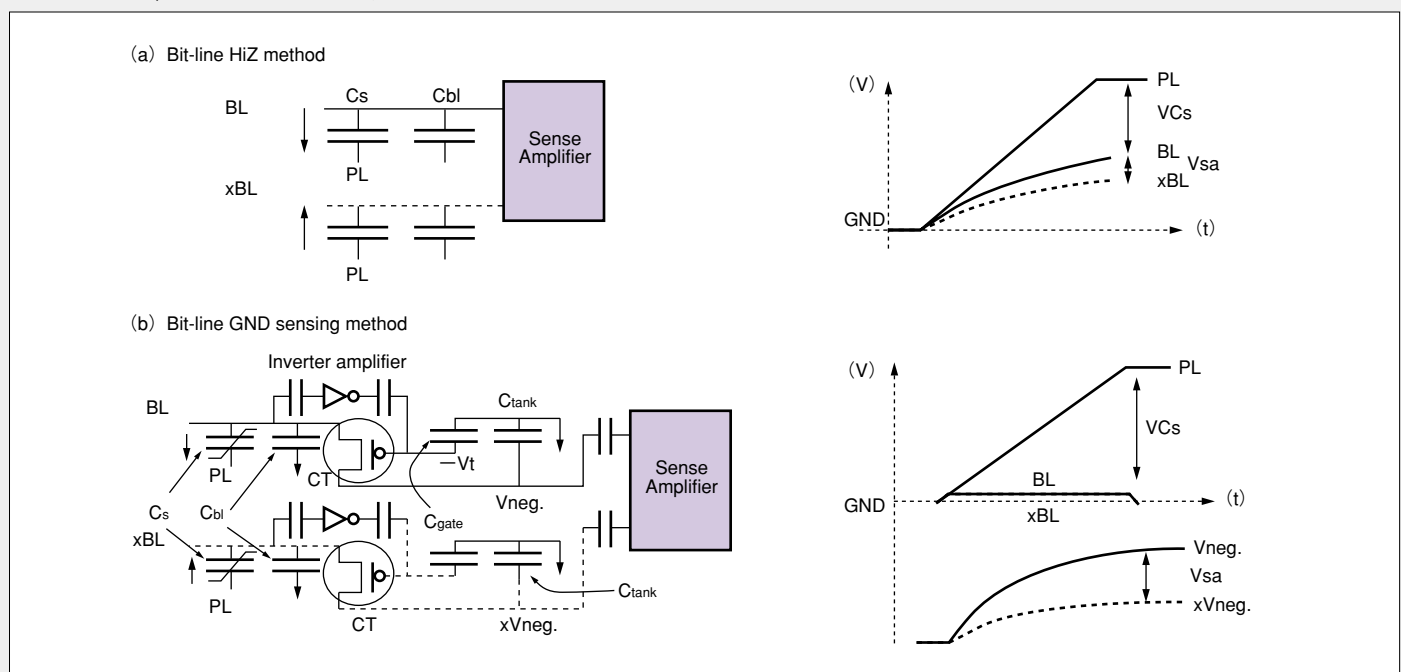
**Fig. 2** shows the hysteresis loop of polarization charge  $Q$  released by the ferroelectric due to the applied voltage. Voltage applied on the ferroelectric capacitor plate line  $V_f$  (V) is plotted on the X-axis of the figure, and the polarization charge for the ferroelectric capacitor  $Q$  ( $\mu\text{C}/\text{cm}^2$ ) is plotted on the Y-axis. As the applied voltage  $V_f$  undergoes the sequential changes  $0\text{V} \rightarrow +\text{VDD} \rightarrow 0\text{V} \rightarrow -\text{VDD} \rightarrow 0\text{V}$ , the ferroelectric charge undergoes the changes point A  $\rightarrow$  point B  $\rightarrow$  point C  $\rightarrow$  point D  $\rightarrow$  point E  $\rightarrow$  point F  $\rightarrow$  point A, thereby forming a hysteresis loop. When the applied voltage undergoes the

change  $0\text{V} \rightarrow +\text{VDD}$ , the ferroelectric charge undergoes the change point A  $\rightarrow$  point B  $\rightarrow$  point C, reversing the polarization state of the ferroelectric capacitor. On the other hand, when the voltage undergoes the change  $+\text{VDD} \rightarrow 0\text{V}$  or  $-\text{VDD} \rightarrow 0\text{V}$ , the ferroelectric charge undergoes the change point C  $\rightarrow$  point D or point F  $\rightarrow$  point A, respectively, leaving the polarization direction of the ferroelectric capacitor un-reversed at a low polarization charge. The polarization charges  $-Q_s$  and  $+Q_s$  at points A and D in Fig. 2 are called the remnant polarization. Points A and D correspond to the “1” and “0” data in the memory cell, respectively. The remnant polarization of points A and D change with different polarization states at  $V_f=0\text{V}$ , even when the voltage to be applied on the ferroelectric film is set to 0V (power supply OFF). Data storing can be possible by the principle like this.

## Problems of Low-Voltage Operation

The sensing margin between “1” and “0” of the ferroelectric memory is detected as the non-switching charge to

**Figure 3** Concept of Bit-Line GND Sensing Method



switching charge difference  $Q_{sw}$ . To ensure a sufficient charge difference, a voltage that saturates the hysteresis loop (points C and F) has to be applied to the capacitor.

**Fig. 3 (a)** shows the conventional bit-line floating reading method (=bit-line HiZ method). The voltage applied on the plate line (PL) during cell read-out is divided into cell capacitor capacitance ( $C_s$ ) and bit-line parasitic capacitance ( $C_{bl}$ ). Since the applied power supply voltage is not applied exclusively to the cell capacitor, a cell capacitor voltage sufficient for reading cannot be ensured. When the power supply voltage is as large as 5V, the voltage required for reading out the "1" and "0" charges from the cell capacitor can be assured even under conditions with potential loss to the bit-line parasitic capacitance division. However, in low-voltage operation at 3V or less, the division loss makes it difficult to obtain sufficient voltage required for data reading. To resolve this problem, FUJITSU has developed a reading method that ensures the application of sufficient voltage even under low voltage\*1.

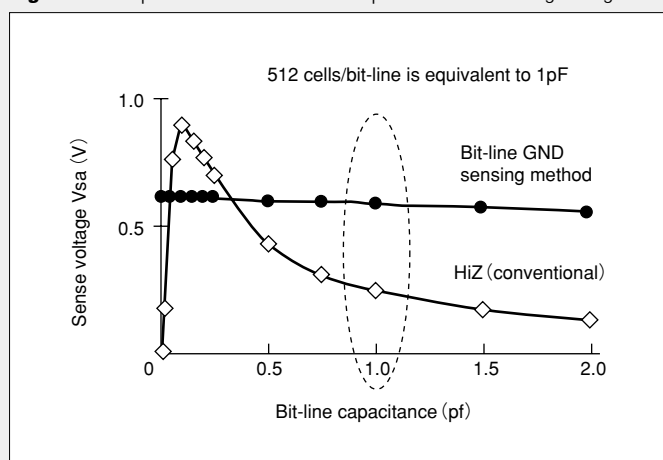
### ■ Concept of Bit-Line GND Sensing Method

In the conventional bit-line HiZ method, the plate-line potential increases during cell read-out and charge flows into the bit-line (BL) (xBL) from the cell (the two bit lines have a relationship of complementary data). The plate-line potential applied at this time is divided into bit-line capacitance  $C_{bl}$  and cell capacitor capacitance  $C_s$ , increasing the bit-line potential. Hence, the voltage applied to the cell capacitor  $V_C$  is less than the voltage applied on the plate-line.

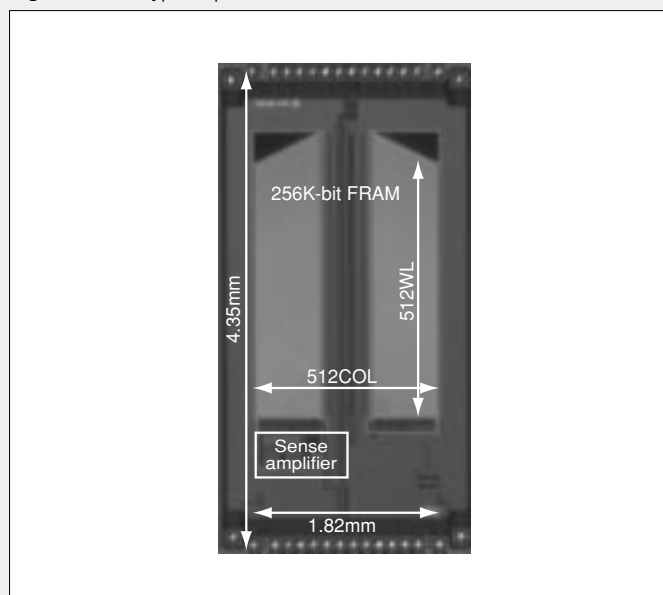
**Fig. 3 (b)** shows the newly developed bit-line GND sensing method. This method consists of the charge transfer (CT) pMOS for controlling the charge supply to the bit-line, the  $C_{gate}$  capacitor for applying the negative potential  $-V_t$  to the charge transfer pMOS gate, and the  $C_{tank}$  capacitor for negative charge accumulation to stabilize the bit-line at GND potential. Circuit operation involves initialization of the gate potential of the pMOS charge transfer to  $-V_t$  during the initial circuit resetting. Next, when the plate-line ascends during cell read-out, the bit-line potential exceeds the GND potential,

supplying the negative charge accumulated in  $C_{tank}$  to the bit-line via the pMOS charge transfer. The bit-line potential to which the negative charge was supplied is stabilized at GND potential at this point. Since the pMOS had a process with small gains in the prototype we developed, feedback was applied using an inverter amplifier in order to firmly stabilize the bit-line at GND potential. By stabilizing the bit-line potential in the proximity of GND, a voltage  $V_C$  close to the power supply voltage could be obtained for the cell capacitor.

**Figure 4** Comparison between Bit-Line Capacitance and Sensing Voltage



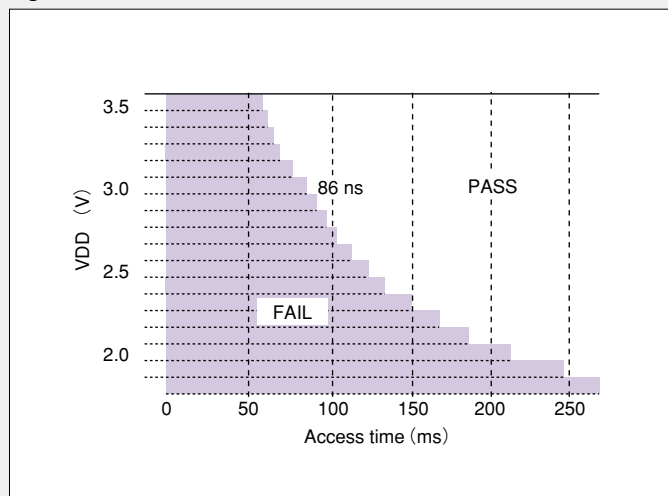
**Figure 5** Prototype Chip



A read-out signal is taken out from the cell capacitor by supplying a negative charge corresponding to the “1” or “0” potential of the memory cell from C<sub>tank</sub>, and then comparing the signal with the increase in V<sub>neg</sub>.

**Fig. 4** shows the relationship between the bit-line capacitance and the voltage difference supplied to the sensing amplifier V<sub>sa</sub> in a simulation comparing the bit-line HiZ method and the bit-line GND sensing method<sup>\*2</sup>. In the bit-line HiZ method, V<sub>sa</sub> rises to a peak against the increase in the bit-line capacitance, and thereafter drops back down to the vicinity of 1/C<sub>bl</sub>. In the bit-line GND sensing method, V<sub>sa</sub> (the difference between BL-side V<sub>neg</sub> and xBL-side V<sub>neg</sub>) stays nearly constant against the increase in the bit-line capacitance, thereby eliminating concerns about the C<sub>bl</sub>/C<sub>s</sub> ratio in calculations to reach an optimal sensing margin in the process of design. The 512 cells bit-line designed in the current FRAM can be used as an example. Here, C<sub>bl</sub> is a point of 1pF. The signal difference V<sub>sa</sub> is 0.24V at this point in the bit-line HiZ method, as opposed to 0.6V, more than double the voltage, in the bit-line GND sensing method. Hence, the bit-line GND sensing method enables data reading in a lower voltage range. Moreover, by allowing designers to develop devices that do not depend on the bit-line length, the bit-line GND sensing method may prove effective as a circuit method for future increases in capacity.

**Figure 6** Access Shmoo (@2MHz, +25°C)



## Prototype Results

**Fig. 5** shows a photo of a 0.35 $\mu$ m FRAM prototype chip employing the bit-line GND sensing method.

- PZT (lead zirconate titanate) capacitor size: 1.4 $\times$ 1.5 $\mu$ m<sup>2</sup>
- 1TIC-type cell area: 7.12 $\mu$ m<sup>2</sup>
- Memory cell: 512 words $\times$ 512 columns, 256K-bit FRAM
- 8 I/O Configuration

**Fig. 6** shows the result of access shmoo measurement. The prototype chip operated at power supply voltage of 3.5V to 1.9V.

- Access time : 86ns (at power supply voltage 3V, 2MHz and room temperature)
- Power consumption: 6mW (at power supply voltage 3V@2MHz)

## Prototype Results

Conventionally, the voltage reduction in FRAM has been impeded by division of the voltage applied on the plate-line between the cell capacitor and the bit-line. In the prototype FRAM using the bit-line GND sensing method, FUJITSU has realized a circuit method that permits the application of the power supply voltage to the memory cell capacitor even at extremely low voltage levels. Once consolidated with logic, the low-voltage operation FRAM will be capable of a wide range of applications in Smart cards. FUJITSU will continue to optimize the circuit as the company works towards the development of a 1.8V power supply voltage operation chip. ★

### [Bibliography]

- \*1: S. Kawashima et al. : A Bit-Line GND Sense Technique for Low-Voltage Operation FeRAM. VLSI symposium on VLSI, 12-3 2001. Session 12-3A.
- \*2: Ali Sheikholeslami et al. : A pulse-based, parallel-element macro model for ferroelectric capacitors. IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control, Vol.47, No.4, p.784-791(July 2000).