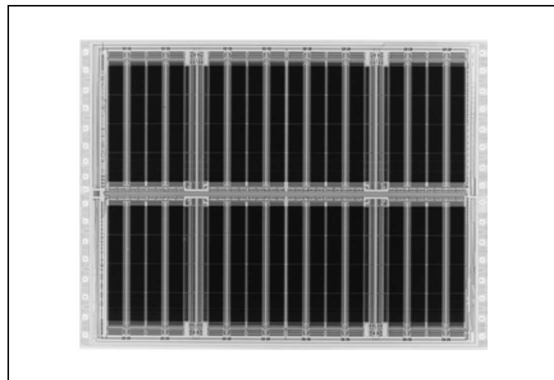
Redundant Circuit Technology and Variable Reference Voltage Circuit Technology for FRAM™

FUJITSU's redundant circuit technology and variable reference voltage circuit technology was selected for an excellence prize at the eighth "LSI Design of the Year" (run by the Handotai Sangyo Shimbun) for its contributions to the commercialization of large-size FRAM™ memory.

Features

- ***Techniques necessary to support 1T1C FRAM™ cell structure***
- ***Redundant cell techniques replace faulty cells***
- ***FRAM™ non-volatile memory use for faulty cell information storage***
- ***Faulty cell identification and storage possible after packaging***
- ***Variable reference voltage increases acceptable cell margins***

Photo 1. External View



Introduction

FRAM™ technology has been actively marketed in recent years. The memory cell configuration currently being used in products is the 2T2C configuration. This consists of two transistors (T) and two ferroelectric capacitors (C). In contrast, 1T1C-type memory cells use half the number of elements and are considered essential for large memory sizes. However, they are very difficult to manufacture, with operating margins less than half those of the 2T2C configuration. This means that practical application of 1T1C has been delayed.

Against this background and with the aim of commercializing 1T1C, FUJITSU has improved its manufacturing processes and determined that a circuit-based approach is necessary to improve yields and achieve more stable operating margins. Accordingly, FUJITSU has developed new redundant circuit technology for improved yields and variable reference voltage circuit technology for more stable operating margins. This article gives an overview of these technologies.

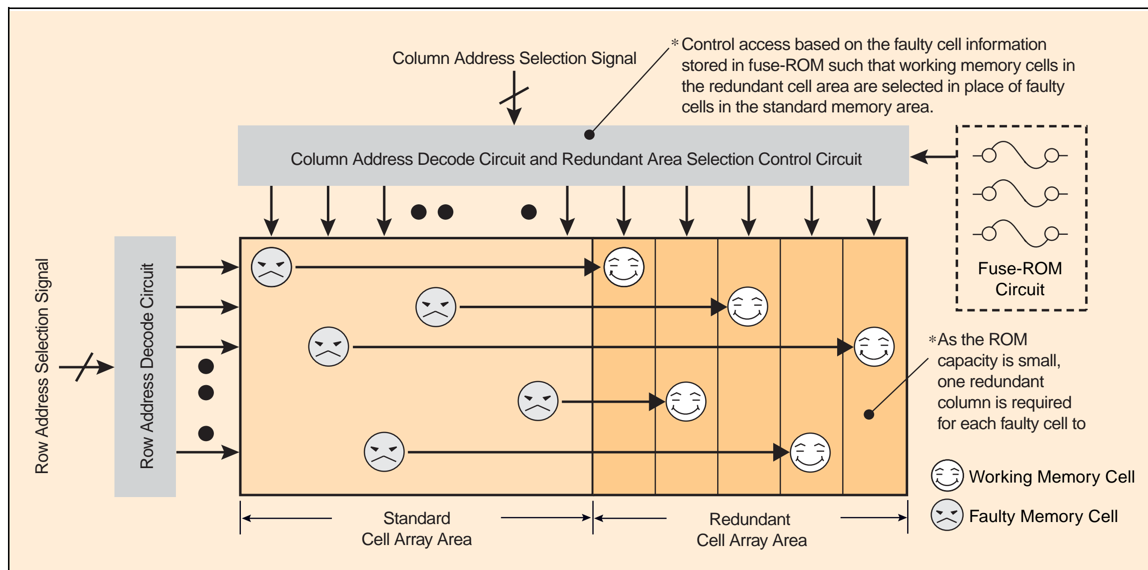
Redundant Circuit Technology

Redundant circuit technology substitutes faulty memory cells with functional cells from a special backup memory array (redundant cell area). The technology represents a circuit-based approach to the problem of low yield, which is inevitable in the production of large-size memory devices and has been used in the past in DRAM, SRAM, and other memory devices.

Figure 1 shows the redundant circuit technology used previously.

In the conventional scheme, the information required from the faulty cells for substitution control is stored in the fuse ROM, which is programmed either electrically or by laser so that the contents are not lost when the power is off. With this approach, providing a redundancy function required additional production steps for the fuse-ROM.

Figure 1. Redundant Circuit Technology Used Previously



This earlier method also substituted a complete backup column for faulty cells in a particular column address, regardless of how many cells were faulty in the original column. That is, the number of backup columns required by this method was equal to the number of faulty cells to be substituted. Accordingly, increasing the ratio of substituted faulty cells required an enlargement of the redundant cell area. However, increasing the size of the redundant cell area also causes the number of faulty cells in the redundant cell area itself to increase. Consequently, there is a limit to how far the ratio of substituted faulty cells can be improved.

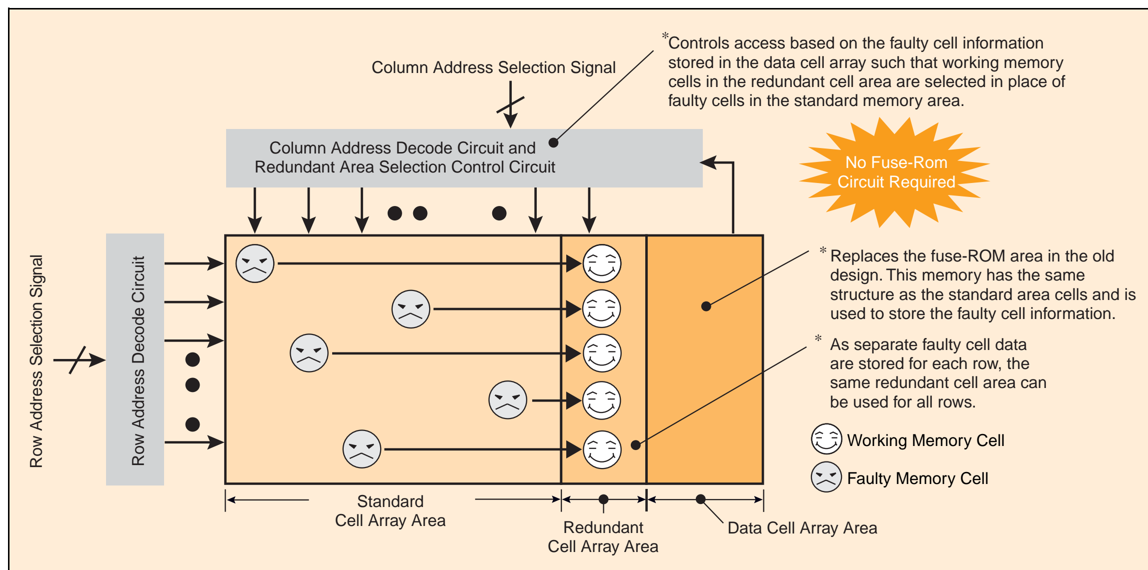
The new technology uses the non-volatile characteristics of FRAM™ memory (stored data is not lost when the power goes off) and uses ferroelectric capacitors to eliminate the fuse-ROM and its associated increase in production cost. Specifically, a third data cell area is added to the existing standard cell and redundant cell areas. The data cell area has the same memory type as the other areas and is used to store the faulty cell information. The faulty cell information is stored independently for each row and is used to control the column direction for the row. That is, if no fault is present in the selected row, the column direction for the standard cell area is selected. If a fault is present, a working cell from the column in the redundant cell area is selected. This row-based control means that a high ratio of faulty cell substitution can be achieved with a small redundant cell area.

"... a high ratio of faulty cell substitution can be achieved ..."

Because this technique does not require a fuse burning step and the associated special equipment, testing costs are also reduced. And because the writing of faulty cell information is performed in the same way as standard writing, writing of fault information is not just restricted to wafer testing. Thus, substitution can also be performed for faults that occur after packaging the chip. Because substitution of faulty cells can be performed using a comparatively simple verification process, it becomes easy to use faulty cell substitution for internal FRAM™ on complex system LSIs.

Figure 2 shows the new redundant circuit technology.

Figure 2. New Redundant Circuit Technology



Variable Reference Voltage Circuit Technology

In the 2T2C cells used in existing FRAM™ products, each cell generates its own reference voltage to determine whether the stored value is “0” or “1”. In contrast, 1T1C cells use a shared reference voltage to detect the stored value. However, variation in this reference voltage causes a deterioration in the read operation margin and is one cause of lower yield. Therefore, ensuring a stable reference voltage is the most important issue in making the 1T1C configuration commercially feasible. In the past, FUJITSU has used a dummy cell with characteristics equivalent to a memory cell to generate the reference voltage, thereby developing circuit techniques that are resistant to process variation.

A further improvement has been added in FUJITSU’s new technology so that the reference voltage can be adjusted by an external test pin during testing. In normal operation, a constant optimum voltage level is generated for the reference voltage. However, during wafer testing, the reference voltage is deliberately varied from the optimum level via external control. This identifies cells with a narrow operating margin, which then can be marked as faulty cells.

“. . . during wafer testing, the reference voltage is deliberately varied . . .”

Simply disabling the faulty cell would only result in the chip being defective, thereby lowering the yield. Instead, the faulty cell is replaced by a cell with an acceptable margin using the redundancy circuit described previously. This minimizes any lowering of yield while reducing the variation in cell characteristics and thereby improving the reliability of the FRAM™ device.

Figures 3 and 4 (see p. 32) show the variable reference voltage circuit technology.

Prototype Chip

FUJITSU has produced a prototype 1 M-bit FRAM™ chip with a 128 KWord x 8-bit configuration that uses 1T1C cells together with the two new circuit technologies described earlier. The 1 M-bit cell array is divided into four blocks with each block having a 32 KWord x 8-bit structure (= 256 K-bit). These blocks are further divided into eight sub-blocks (4 KWord x 8-bit), and each sub-block has one column of redundant memory cells. With this configuration, the increase in cell array size due to the addition of the data cell area is approximately 5%, but this has resulted in a substitution ratio that is one to two points higher than before.

The process technology used for the chip is 0.5-μm rule, two-layer metal process, with PZT used as the ferroelectric material. PZT is currently the standard material used for ferroelectric elements. The memory cell size is 15.8 μm^2 and the chip size is approximately 48.3 mm^2. The standard power supply voltage is 5.0V, and the chip has a guaranteed access time of at least 80 ns.

Product Features

- Process technology: 0.5 μm two-layer metal, PZT used for ferroelectric elements
- Memory configuration: 128 KWord x 8-bit
- Memory cell size: 3.95 μm x 4.00 μm = 15.8 μm^2
- Ferroelectric capacitor size: 1.1 μm x 2.75 μm = 3.025 μm^2
- Chip size: 5.7 mm x 8.47 mm = 48.279 mm^2
- Power supply voltage: 5.0V (standard)
- Read speed: 80 ns (max.)

Future Developments

Although the prototype used the 0.5-µm process, the new circuit technologies can also be used with next-generation process technologies. FUJITSU will continue to work toward the commercialization of low-cost, large-capacity FRAM™. ◆

Figure 3. Variable Reference Voltage Circuit Technology (1)

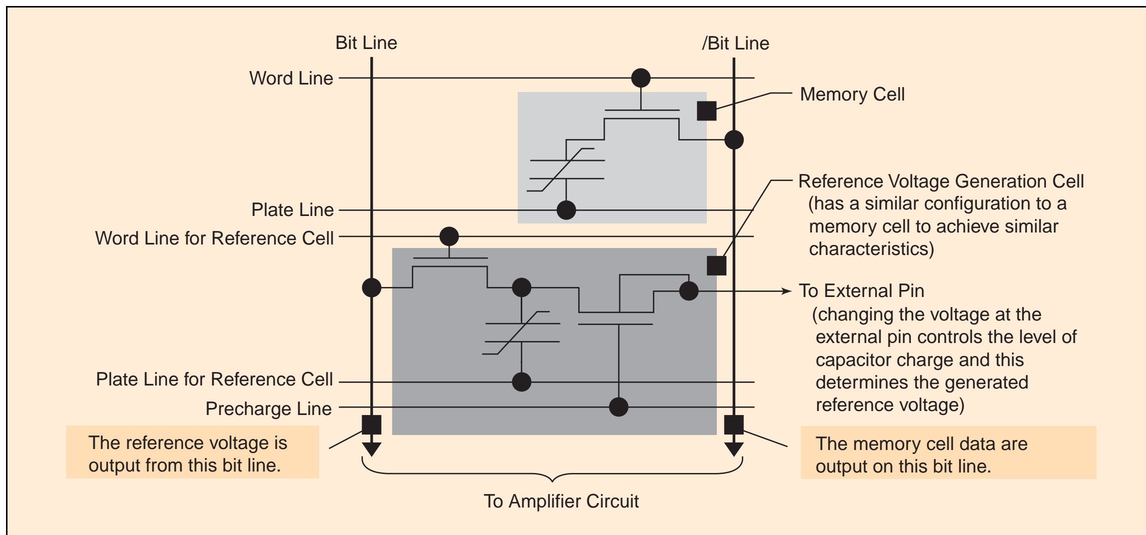


Figure 4. Variable Reference Voltage Circuit Technology (2)