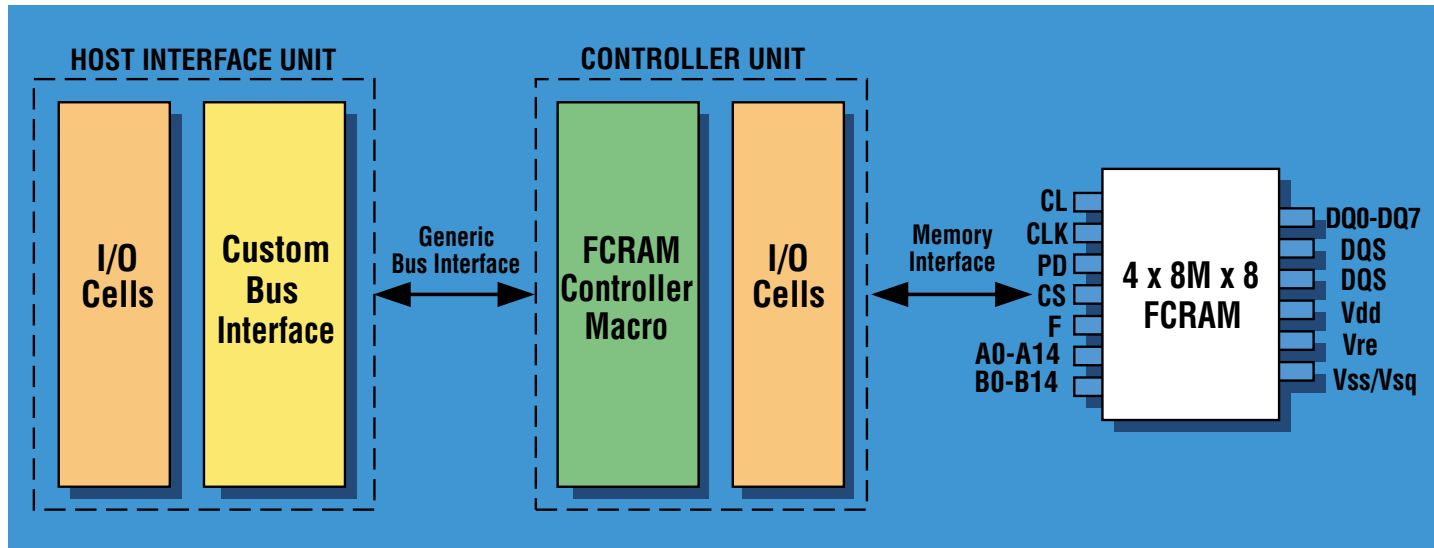


Synthesizable High Performance FCRAM™ Controller



► Features

- Modular Design
- CPU Programmable for Various Modes of FCRAM Operation
- Programmable CAS Latency (CL)
- Programmable Burst Length (BL), Burst Type (BT)
- Programmable Refresh Count Register
- Programmable Power-on Initialization Duration
- Automatic Power-on initialization
- Ability to transfer data between the controller and the FCRAM in quad word

► Benefits

FCRAM Controller used in conjunction with Fujitsu FCRAM provides the following benefits:

- Enhances throughput in systems approaching 200MHz and beyond where cache misses are occurring more frequently
- Can be used to buffer large blocks of data in network applications
- Easily configurable to support customer's memory systems
- Allows customers to specify/build their own bus interface

Synthesizable High Performance FCRAM Controller

► Description

Fast Cycle RAM (FCRAM) provides a significant improvement in memory bandwidth. FCRAM enhances throughput in systems approaching 200 MHz and beyond where cache misses are occurring more frequently.

The design of the FCRAM Controller enhances system throughput similar to that of the DDR SDRAM system. The enhancement is based on the time saved while pipelining commands thus reducing random memory access time.

The FCRAM Controller contains two basic interfaces.

- 1) Generic bus interface which provides an interface to an application.
- 2) Memory interface that connects to a location belonging to an FCRAM memory system.

A custom bus interface module can be built to connect the generic application bus to ARM AHB or Fujitsu FOIP (Fast optimized IP) Bus developed to work with the ARC Processor.

The Controller unit acts as slave and thus its response is fed back as slave response to a master interface through the custom bus interface block. There are two main blocks of the Controller unit. The first block, the FCRAM Controller macro block, takes inputs from the host interface unit (master) and converts the transaction requests to FCRAM commands. The second block is the I/O cells block which handles the tri-state in/out busses, strobes and enable signals that control the input and output data.

This macro can be used in a variety of applications:

- High-end networking equipment for the WAN and LAN applications
 - Router
 - Switches
 - Line cards
- High-end Servers

► Deliverables

The Fujitsu value-added FCRAM Controller Macro enables customers to design a variety of complex system-on-a-chip ASIC designs for high-end networking applications.

A Fujitsu application engineer works with the customer to identify the customers' specific memory and other IP requirements. Fujitsu provides the customer with the

following information to support the FCRAM Controller macro:

- Encrypted Verilog RTL Simulation model
- Encrypted Verilog Test bench
- Gate level netlist
- User's Guide

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Printed in the U.S.A. ASIC-FS-20879-09/2001