0.18µm CMOS Process (CS80A)

Features

- 2-Poly and 6-Metal Process
- Retrograde Twin Wells on P Epi Substrate
- STI(Shallow Trench Isolation)
- Salicided Gate
- Salicided Source and Drain
- CMP Planarization
- CVD Filling for Via
- Stackable Contact and Vias
- Oxide/Nitride Passivation

Design Rules

Layer	Width	Space	Unit
Diffusion	0.22	0.24	µm
Poly	0.18	0.24	µm
Contact	0.28	0.26	µm
Metal 1	0.26	0.28	µm
Via 1	0.28	0.26	µm
Metal 2	0.26	0.28	µm
Via 2	0.28	0.26	µm
Metal 3	0.26	0.28	µm
Via 3	0.28	0.26	µm
Metal 4	0.44	0.46	µm
Via 4	0.44	0.46	µm
Metal 5	0.44	0.46	µm
Via 5	0.44	0.46	µm
Metal 6	0.44	0.46	µm

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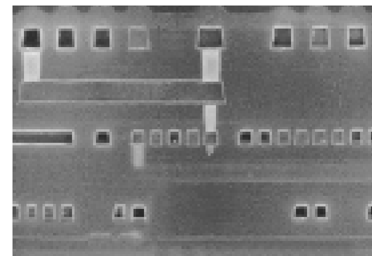
Device Technology			
Supply Voltage	1.8V		
Gate Oxide	4nm		
	NMOS	**PMOS**	**Unit**
Vth	0.53	-0.48	V
Idsat	0.56	-0.24	mA/μm

Option	
Thick Gate Oxide Tr.	For 3.3V
Diffusion Resistor	1.6kΩ/sq
Bulk-Poly Capacitor	2.47fF/μm²
Poly-Poly Capacitor	1.38fF/μm²
Triple-well	Available

Interconnect Technology		
	Metallization	**Resistance**
Gate	Salicided Poly	6Ω/square
S&D	Salicided S/D	6Ω/square
Vias Filling	CVD	
Stacked Vias	All	
Planarization	CMP	



Cross Section

Device Performance			
	Transistor	Gate	Unit
Density	342	86	K/mm²
	Inverter	2-NAND	Unit
Gate Delay	24	39	ps
SRAM Cell Size		4.9μm²	
SRAM Speed (taa)		1.3 ns	

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