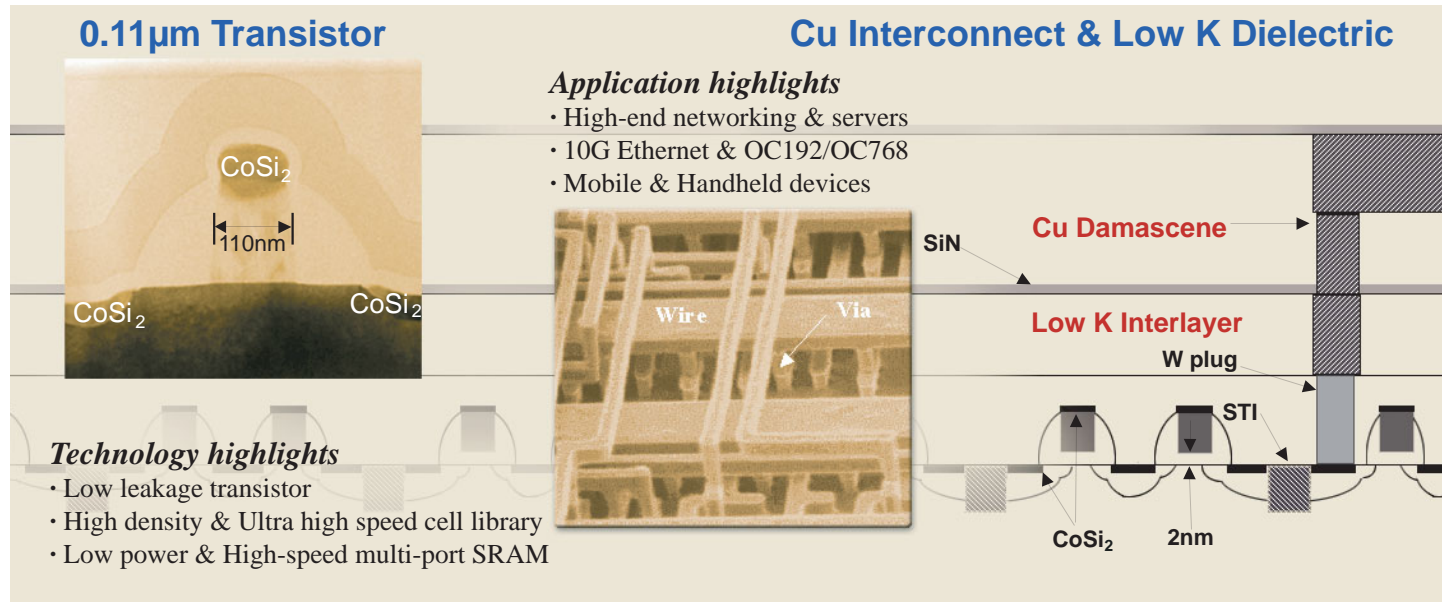


0.11 μ m CMOS Standard Cell

CS91 ASIC Series



► Features

Technology

- 70nm effective channel length
- Low resistive Cu interconnect for high performance
- Low-K dielectric to reduce parasitic capacitance

Cell Library

- Four cell libraries to provide design flexibility and tradeoff between ultra high performance and low standby power
- Very high density: 200K raw gates/mm²
- High-density diffused RAMs and ROMs
- High-speed mixed-signal macros
- Analog PLLs

High Speed & Standard I/Os

- 2.5G to 3.125G I/Os
- OIF & XAUI Standards
- Standard I/Os: LVTTTL, SSTL, HSTL, LVDS, P-CML

Application Specific IPs & IPWare™ Support

- Computational Cores: ARM, ARC, DSP, multi-channel VOIP
- Controller Cores: ARM cache, FCRAM™ Controller
- Connectivity Cores: USB, PCI, I²C, Ethernet, 1394

Wide Variety of Packaging

- Flip Chip BGA: 450 to 2,116 pins, designed for high-speed I/Os
- Enhanced BGA, TAB BGA, Fine Pitch BGA, Plastic BGA, QFP & HQFP

Design Methodology & Supports

- Methodology in place to support multi-million gates hierarchical designs
- Excellent design center support at San Jose, Dallas and Raleigh
- Worldwide service organizations for global support

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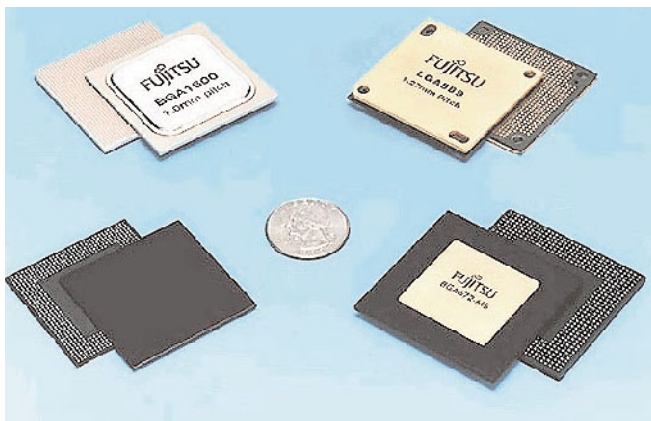
Description

Fujitsu's CS91, a 110nm (70nm Leff) standard-cell product, is based on Fujitsu's state-of-the-art CMOS process technology, a deep sub-micron process designed for today's high-speed and low-power SOC products. The cell library, which is optimized for synthesis-based designs, has accurate timing and power-characterized data, cell areas, and statistical wire-load models. The CS91 standard-cell library contains both high-performance and high-density cells, giving designers the option of combining both types of standard cell blocks on the same chip. The CS91 library supports popular third-party tools and data-exchange file standards. The CS91 chip cores can operate at 0.8V to 1.3V range. The I/Os, operating at 0.8V to 3.6V range, can conveniently interface with various types of devices. Interface options include low-swing, high-speed I/Os and high-speed bus interface I/Os.

Also provided in CS91 are high performance and area-optimized memories, mixed-signal blocks, analog functions, a rich set of IP Cores and Mega Macros, and various I/O interfaces.

CS91 Standard Cells in four discrete library flavors

- CS91HU (Ultra High Speed transistor) for applications requiring ultra high performance
- CS91HZ (High Speed transistor) for applications requiring high performance at low power
- CS91HN (Normal transistor) for applications requiring high performance with low leakage
- CS91SN (Normal transistor) for high density with low power applications



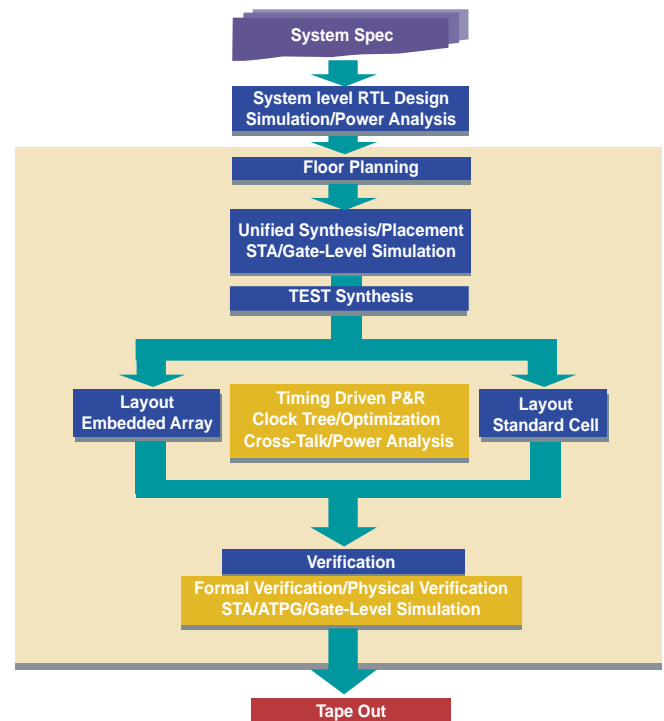
Packages for 0.11 μ m ASIC products

Fujitsu advanced Flip Chip BGA packages are specially

designed for high-speed back plane applications using 2.5G to 3.125G I/Os. Besides FCBGA packages, Fujitsu Advanced Packaging also offers traditional QFP and Heat-spreader QFP packages, TAB-BGA, Enhanced BGA (EBGA) and Fine-pitch BGA (FBGA) packages in various pin/ball pitch and in wide range of pin-count.

Design Methodology

Fujitsu's design methodology ensures first-time silicon



System LSI Design Flow

success by integrating proprietary point tools with popular, sign-off-quality CAD tools such as:

- Automatic IO frame generator & packaging rule checker
- Test insertion, ATPG and ATE simulation
- Memory compiler
- Logic & test design rule checker
- Power analysis & optimization
- High-precision library characterization & Delay calculator
- Quasi 3-D parasitic extraction tool

Fujitsu's clock-driven design methodology is devised for low power and low skew. The methodology identifies the best-suited clock distribution strategy for a given design and predicts performance in advance. Fujitsu supports

0.11 μ m CMOS Standard Cell

co-simulation, emulation and high-level floor planning to optimize the power, timing, and size of the design. This enables the designer to make effective architectural-level decisions to achieve optimal design solutions. Fujitsu's design-for-test strategy includes boundary scan (JTAG) and full and partial scan, as well as a built-in self-test for both logic and memory.

Memory Macros and Compilers

Memory Type	
High-Density 1RW - RAM	(max. 256k-bit)
High-Speed 1RW - RAM	(max. 256k-bit)
1RW - RAM (PW)	(max. 256k-bit)
2RW - RAM (PW)	(max. 256k-bit)
1RW1R - RAM (PW)	(max. 256k-bit)
ROM	(max. 512k-bit)
Very Large 1RW - RAM with redundancy	(max. 4M-bit)
Low Power 1RW - RAM	(max. 512k-bit)
1RW - RAM (BUS & PW)	(max. 512k-bit)
High-Speed 2RW - RAM	(max. 256k-bit)
Register File 2R1W	(max. 4.6k-bit)
Register File 2R2W	(max. 4.6k-bit)
FIFO	(max. 16k-bit)
Delay Line	(max. 64k-bit)

PW - partial write

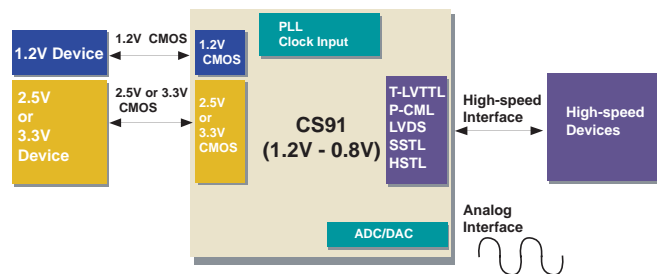
Phase-Locked Loops

- Analog: up to 3.2 GHz
- DLL

I/O: High-speed and conventional

- 2.5V and 3.3V CMOS
- High-speed transceivers P-CML, LVDS, SSTL, HSTL & GTL
- PCIX, RapidIO & HyperTransport
- 622Mbs/1.25Gps/2.5Gbs CDR/Serdes
- 3.125Mbs XAUI, SFI4-II, SFI-5 with dynamic deskew

CS91 I/O Interface Capabilities



SOC IP Cores

- Networking & Communication
POS- PHY Level 3 & Level 4, OC3 & OC12 Sonet Framer
Utopia I/ II, 10/ 100 MAC
- Processors & DSP
ARC3 & ARC4 (+ DSP), ARM9
- Std. Bus Controllers & Bus Bridges
USB(1.1) Device/Host Controller, USB2.0 PHY
PCIX, PCI (2.1) - 33MHz, 66MHz & PCI Host Controller
1394 Link & PHY - 400 Mbps
- Multimedia Access & Wireless
VoIP core, AC97 controller, JPEG, MPEG, Video encoder
Bluetooth, 802.11a, 802.11b
- Memory Controllers
ARM Cache, FCRAM, SDRAM, DDR Controller
- ARM & Other Peripherals
Various ARM peripherals
DMA Controller (8 Ch), UART, Interrupt Controller, I²C

More IPs are being added

Applications

Market	Typical Application
High-end LAN/WAN	Routers, switches, High-end servers, storage
Wireless	Cellular handsets, PDAs, Global Positioning Systems
Access	Network storage, Digital set-top box & modem, Home Gateway

Multiplier Compiler

- Multiplicand (m): $4 \leq m \leq 32$
- Multiplier (n): $4 \leq n \leq 32$

0.11 μ m CMOS Standard Cell

ASIC Design Kit and EDA Support

Supported CAD Tools (1)

Function	Tool
Logic Synthesis	<ul style="list-style-type: none"> • Synopsis Design Compiler, Power Compiler • Cadence BuildGates
Simulation	<ul style="list-style-type: none"> • Synopsys VCS, VSS • Cadence Verilog-XL, NC Verilog, NC-VHDL • Mentor Graphics ModelSim
Power Analysis	<ul style="list-style-type: none"> • Synopsys DesignPower • Sequence Design PowerTheater • Fujitsu Pscope, SilicoScope
Floor Planning	<ul style="list-style-type: none"> • Cadence First Encounter, Design Planner • Cadence Integration Ensemble

Supported CAD Tools (2)

Function	Tool
Physical Synthesis	<ul style="list-style-type: none"> • Synopsis Physical Compiler • Cadence Silicon Ensemble-PKS • Magma Design Automation Blast Chip
Clock Synthesis	<ul style="list-style-type: none"> • Cadence CTGEN
Place & Route	<ul style="list-style-type: none"> • Cadence Silicon Ensemble • Fujitsu GLOSCAD
STA	<ul style="list-style-type: none"> • Synopsys PrimeTime • Fujitsu GISTA
Physical Optimization	<ul style="list-style-type: none"> • Cadence First Encounter, Silicon Ensemble-PKS • Sequence Design PhysicalStudio

Supported CAD Tools (3)

Function	Tool
Test Synthesis/ATPG	<ul style="list-style-type: none"> • Fujitsu ATREX, FANTCAD, RAPARA • LogicVision Logic BIST, Memory BIST
Formal Verification	<ul style="list-style-type: none"> • AVANT! Design VERIFYer • Verplex Tuxedo-LEC • Fujitsu Assure
Physical Verification	<ul style="list-style-type: none"> • Cadence Dracula, Assura • Mentor Graphics Calibre
Memory Compiler	<ul style="list-style-type: none"> • Fujitsu BankBase

CS91 Maximum Ratings

Parameter	Symbol	Maximum Ratings	Unit	
Supply voltage	1.2v (typ.)	VDD	-0.5 to +1.35	V
	2.5v (typ.)	VDD	-0.5 to +3.6	
	3.3v (typ.)	VDD	-0.5 to +4.6	
Input voltage	VI	-0.5 to VDD+0.5	V	
Storage temperature	Plastic	TST	-55 to +125	degC
	Ceramic	TST	-65 to +125	
Junction temperature	Tj	-40 to +125	degC	

Mixed Signal Macros

- A/D Converters
 - 8-bit & 10-bit
 - 1MS/s to 80MS/s
- D/A Converters
 - 8-bit, 10-bit & 12-bit
 - 200KS/s to 200 MS/s
- Analog macros
 - Op-amps, Bias, Switches
 - Comparators, BGR

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 Printed in the U.S.A. ASIC-FS-20909-3/2002