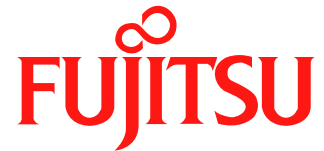


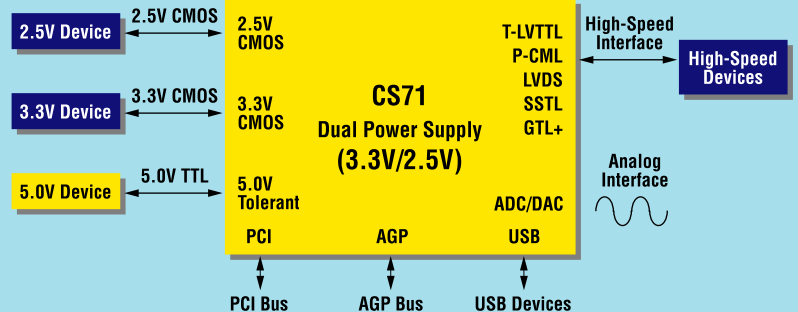
# CS71 Series Standard Cell

0.25 $\mu$ m CMOS Technology



## Features

- 0.18 $\mu$ m  $L_{eff}$  (0.24 $\mu$ m drawn)
- Up to 10 million gates
- 0.05 $\mu$ W/gate/MHz power dissipation
- 2.5V, 3.3V, 5V tolerant I/O options
- Special high-performance I/Os—PCML, LVDS, PCI, SSTL, GTL+, AGP, USB
- Core power supply voltage: 2.5V, 1.8V, 1.5V
- Junction temperature: -40°C~125°C
- High-performance embedded SRAM and DRAM
- Analog and digital PLLs
- Powerful mixed-signal offering—A/D and D/A convertors
- Advanced packaging
- Proven design methodology and tool support



## Description

Fujitsu's CS71, a 0.25 $\mu$ m (0.18 $\mu$ m  $L_{eff}$ ) standard cell product, is based on Fujitsu's state-of-the-art CMOS process technology—a process designed for high performance and high integration. The CS71 family offers up to 10 million gates, using as many as five layers of metal.

The CS71 standard cell library is one of the most aggressive and enhanced libraries for implementing today's deep submicron system-on-silicon designs. The cell library is optimized for synthesis-based designs, and is designed for low power.

The core process operates at 1.5V, 1.8V, and 2.5V, with I/Os operating at 2.5V, 3.3V, or 5V tolerant conditions.

The library supports the most popular third-party tools and data exchange file standards.

Both standard and staggered I/O pad configurations are available at 44 $\mu$ m, 66 $\mu$ m and 88 $\mu$ m pad pitches. Interface options include low-swing, high-speed I/Os and high-speed bus interface I/Os.

In addition to the traditional QFP packages, the CS71 family is available in Ball Grid Array.

CS71 offers a rich set of ADCs and DACs, digital and analog PLLs, high-speed RAMs, ROMs, and DRAMs, as well as a variety of other embedded functions.

## Design Methodology

Fujitsu's design methodology ensures first-silicon success by integrating proprietary point tools with the most popular, sign-off quality, industry-standard CAD tools.

Fujitsu's clock-driven design methodology is devised for low power and low skew. It identifies the best-suited clock distribution strategy for a given design and predicts performance in advance. Fujitsu supports co-simulation, emulation, and high-level floorplanning to ease the power, timing, and size estimation of the design. This enables the designer to make effective architectural-level decisions to achieve optimal design solutions.

Fujitsu's design methodology supports cycle-based simulators and formal verification, as well as static timing analysis and the more conventional VHDL and Verilog simulators. Fujitsu's design-for-test strategy includes boundary scan (JTAG), full and partial scan, as well as a built-in self-test for memory.

## Applications

CS71 offers high integration and performance and low-power consumption. High performance transmission and switching applications, as well as power-sensitive applications, such as mobile computing and mobile communications, can benefit from this technology.

# CS71 Series Standard Cell

## Mixed-Signal Macros

### D/A Converters

- **10-bit:** 1 MS/s, 1.5 MS/s, 30 MS/s, 50 MS/s, 100 MS/s, 220 MS/s
- **8-bit:** 200 KS/s, 1 MS/s, 50 MS/s

### A/D Converters

- **12-bit:** 1 MS/s
- **10-bit:** 1 MS/s, 20 MS/s, 40 MS/s
- **8-bit:** 1 MS/s, 30 MS/s, 50 MS/s
- **6-bit:** 100 MS/s, 500 MS/s

## Memory Macros

- **SRAM Compiler:** single and dual port (1 R/W, 1R), up to 72K bits per block, both BUS and Partial Write
- **ROM Compiler:** up to 512K bits per block
- **High-density single-port RAM** 288K bits
- **Register file (2R/W, 2R/2W), up to 4,608 bits**

## Phase-Locked Loops

- **Analog:** up to 250 MHz (622 MHz under development)

## I/Os

- 2.5V, 3.3V, and 5V tolerant
- Slew-rate controlled
- CMOS, TTL, PCML, T-LVTTL, LVDS, PCI, SSTL, GTL+, AGP, USB

## SOC IP Cores

ARM 7TDMI Hard Macro  
 ARC 32-bit RISC  
 834/836 SPARClite Hard Macros  
 Oak DSP Hard Macro  
 10/100 MAC  
 64/256 QAM  
 MPEG2 Decoder/Demultiplexer  
 8VSB TV Demodulator  
 AC-3 Dolby Voice Decoder  
 JPEG Encoder and Decoder  
 PCI-33/66 MHz, 32/64-bit cores  
 USB Host Controller/Device  
 I<sup>2</sup>C  
 IDE (ATA3) Host Controller  
 Smart Card I/F  
 IRDA I/R Interface  
 More IPs are being added

## ASIC Design Kit and EDA Support

Verilog Logic Simulators from Cadence, Synopsys, and Mentor	Verilog-XL, NC-Verilog, VCS, Model-sim (Verilog)
VHDL/VITAL Logic Simulators from Synopsys, Cadence, and Mentor	VSS, Model-sim (VHDL), V-System, Leapfrog
Synthesis, power, DFT, and STA tools from Synopsys	Design Compiler, Design Power, Test Compiler, PrimeTime, MOTIVE, and Sunrise TestGen
Other EDA tools	Chrysalis Design Verifier and Sente Watt Watcher

## PACKAGE AVAILABILITY

No. of Pins	Frame Size
<b>Thin and Low Profile QFP Packages (0.4, 0.5 mmlead pitch)</b>	
100	K1, K2
120	K2, K3
144	K3, K4, K8, T2, T3
176	K4, K5, T3, T4
208	T4, T5, T6, T7, T8, T9
256	T8, T9, TA, TB, TC
<b>Shrink QFP Package (0.5 mmlead pitch)</b>	
176	J1, J2, K4, K5
208	J3, J4, J5, K5, K6, K7, K8
240	J4, J5, J6, K6, K7, K8
<b>Heatspreader QFP Package (0.4, 0.5 mmlead pitch)</b>	
208	J3, J4, J5, J6, J7, J8, J9, K5, K6, K7, K8 T4, T5, T6, T7, T8, T9
240	J4, J5, J6, J7, J8, J9, JA, K6, K7, K8, T6, T7, T8, T9, TA
256	J5, J6, J7, J8, J9, T7, T8, T9, TA, TB, TC
304	J7, J8, J9, JA, JB, JC, JD, JE, JF, JG, TB, TC, TD, TE, TG
<b>Ball GridArray (1.27 mmball pitch)</b>	
256	J3, J4, T7, T8, T9, TA, TB
352	J6, J7, J8, TB, TC, TD
420	J8, J9, TD, TE
576	JA, JB
672	JC, JD
<b>Fine-Pitch Ball GridArray (0.75, 0.8 mmball pitch)</b>	
144	T3
176	T3, T4
224	T5, T6, T7, T8, T9
288	T8, T9, TA, TB, TC
<b>Tab Ball GridArray (0.8, 1.0 mmball pitch)</b>	
304	L4, L5
352	L5, L6, L7
480	L6, L7
560	L7, L8, LB, LC
660	L8, L9
720	L9, LA, LB, LC, LD, LE

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