

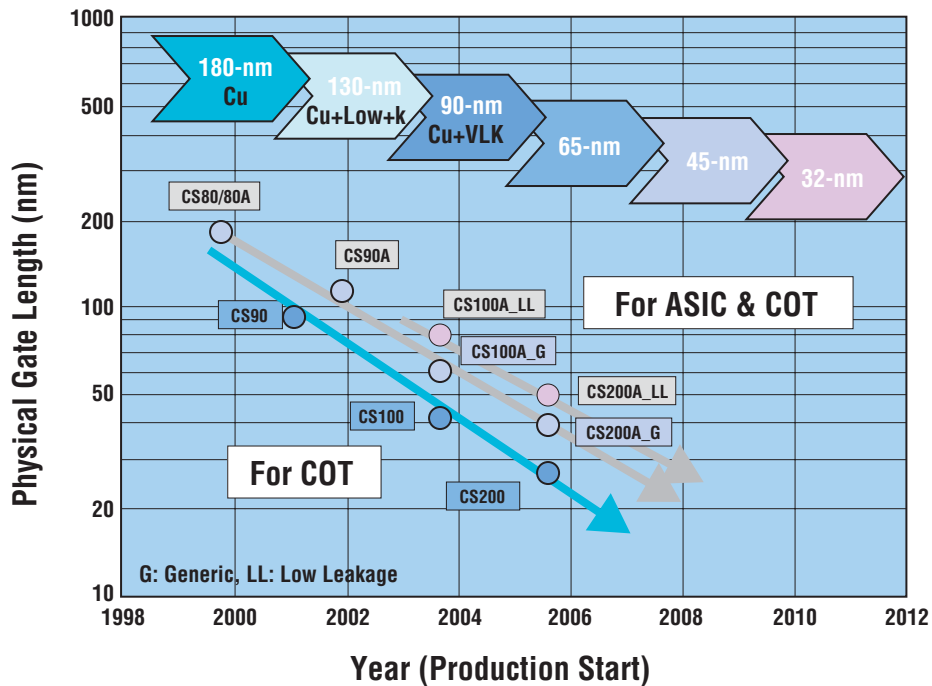
90nm node CMOS Process (CS100A)

Features

Technology Code	CS100A_HP		CS100A_G			CS100A_LL		
Transistor	UHS	HS	UHS	HS	STD	UHS	HS	STD
Physical Gate Length (nm)	60	60	60	60	60	80	80	80
Gate Oxide Thickness (nm)	1.9	1.9	2.5	2.5	2.5	2.7	2.7	2.7
Supply Voltage (V)	1.0	1.0	1.0	1.0	1.0	1.2	1.2	1.2
NMOS Ids (μA/μm)	910	640	740	630	480	820	715	450
PMOS Ids (μA/μm)	-410	260	-330	-280	-200	-395	-320	-200
NMOS Ioff (nA/μm)	50	1	30	5	0.5	30	3	0.01
PMOS Ioff (nA/μm)	-50	-2	-30	-5	-0.5	-30	-3	-0.01
Gate Leak Current Nch(nA/μm)	50	50	0.5	0.5	0.5	0.02	0.02	0.02
Gate Leak Current Pch(nA/μm)						-0.004	-0.004	-0.004
Basic Gate Delay (ps)	9	11	<10	<13	<20	11	13	22
Number of Available Poly Layer	1							
Number of Available Metal Layer	10Cu+1Al							
Via Filling	Cu Dual Damascene							
ILD Structure	Full Low-k							
SRAM Cell Size (μm ²)					1.07	1.14		
Dual Gate Oxide Options	Available							
Mixed Signal Options	Available							
RF Elements	MIM cap., Poly Resistor, Inductor							
Fuse	RAM Redundancy							

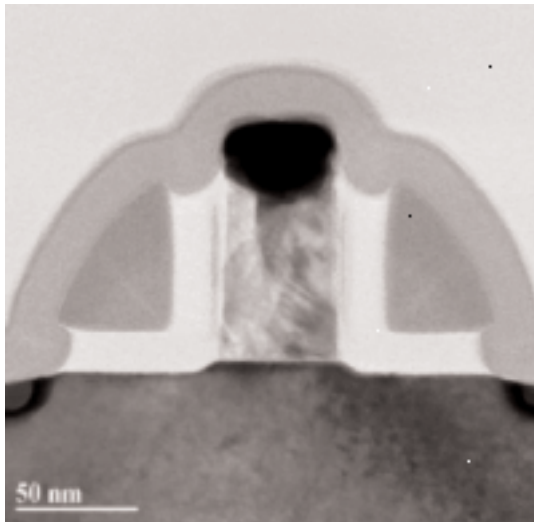


Technology Roadmap

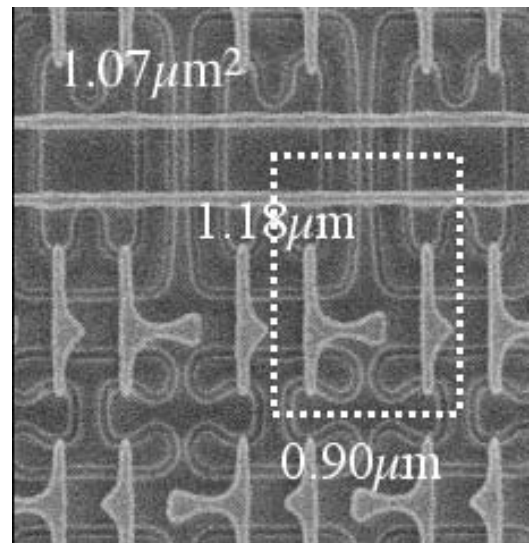


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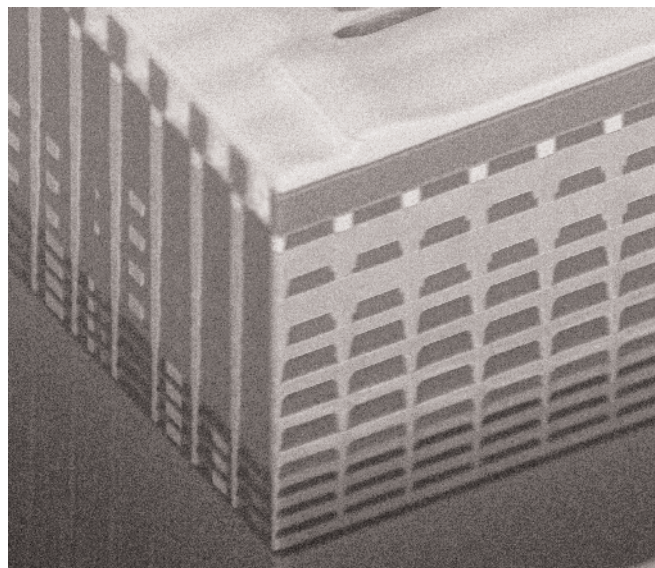
Transistor



SRAM



Interconnect



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