

## ASIC Solutions

### AccelArray™ Technology Reduces ASIC Costs and Turnaround Times, and Offers 400 Mbps DDR Interface

by Simone Shaghafi, ASIC Marketing Manager, Fujitsu Microelectronics America, Inc.

**New** ASIC design architectures dramatically reduce product development costs and time-to-market, providing far more performance than field programmable arrays (FPGAs). Called “Platform ASICs” by some suppliers and “Structured ASICs” by others, the architecture is ideal for mid-volume networking, storage, communications, and emerging consumer electronics designs such as digital TVs. With turnaround times reduced to as few as 6 to 10 weeks from 18 months for many applications, Platform ASICs also apply design reuse whenever possible, and can be adapted to fast-moving changes in customer demands or requirements. Fujitsu Microelectronics America (FMA) recognizes the leadership of Synplicity® in delivering EDA tools to companies developing Structured and Platform ASICs

#### AccelArray Benefits

AccelArray, Fujitsu's innovative semiconductor “structured platform” and design environment, saves cost and time because its platforms come with pre-defined, pre-verified, and pre-diffused layers to which customers can add their differentiations – often proprietary logic – in available metal layers. A typical configuration among the earliest platform ASIC designs offers two “customizable” metal layers, but with more advanced process technologies like 0.11 micron and 90-nm, more metallization layers are available, and a higher number of layers are used to improve routing congestions and resource utilization. AccelArray technology offers 4 to 5 metal layer customizations in 0.11-micron process technology, along with providing a significant time-to-market advantage.

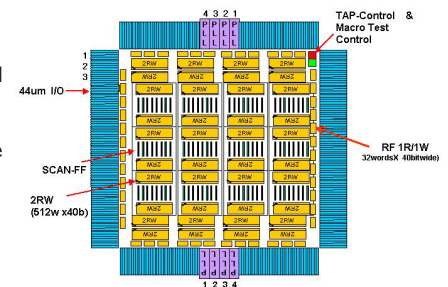


Figure 1 AccelArray Modular Architecture

#### AccelArray Architecture

The AccelArray architecture eliminates the most tedious and time-consuming design tasks such as memory insertion, test development and insertion, and power-mesh design and analysis (Table 1). Complex tasks such as I/O timing closure are easily completed.

#### Interface Trends

The choice for the interface I/O falls into three categories. When the interface speed is below 150 Megabits per second (Mbps), a full synchronized scheme is used with a Single DRAM (SDRAM) interface. Currently, source synchronous interfaces are used with DDR-DRAM, QDR I/II – DRAM and RLDRAM when throughput is less than 1 Gigabit per second (Gbps). In applications where greater than 1 Gbps is needed, embedded clock or Clock Data Recovery (CDR) macros are used.

#### AccelArray Supports Virtually all Types of DDR Interfaces

When designing Double Data Rate (DDR) interfaces, ASIC developers are faced with the difficult challenge of timing closure between the receiver and the transmitter sides. With a speed of 400Mbps and timing margins of 2.5ns, small jitter and skew from 64 to 90 individual data channels are required.

Fujitsu's AccelArray also incorporates support for the largest variety of memory interfaces, a major requirement in an increasing number of applications. These interfaces include DDR, Synchronous DRAM, RLDRAM, and Fast Cycle RAM (FCRAM). More than 50 percent of all available I/Os in the AccelArray technology can support the DDR interface up to 400 Mbps.

The AccelArray technology provides a predefined DDR macro that can support low jitter and skew by implementing design techniques. The transmitter (TX) and receiver (RX) sides are each designed to reduce the skew between outgoing and incoming parallel data signals.

Design Task	AccelArray	Standard Cell
DFT insertion	Not necessary	Necessary
IR-drop analysis	Not necessary	Design/verification
Clock-tree synthesis	Not necessary	Necessary
Internal timing closure	Setup	Setup/hold/test
I/O timing closure	Interface module provided	Complex
X-talk analysis/fix	Data nets	Clock/data/test nets

Table 1

### DDR Interface is a Source Synchronous Interface

In source-synchronous applications, data is transferred with the clock. This requires the clock and data to have the same propagation delay. With SDR memory, data is transmitted during one clock cycle and, with DDR memory, two data bits are transferred with one clock cycle.

The DDR interface requires the same switching rate between the source synchronization clock and transfer data. DDR requires no upgrades to the existing transmission line, yet offers a performance boost over the Single Data Rate (SDR) interface. This is perhaps the most important reason behind the wide adoption of DDR memory.

### AccelArray DDR Modules Support 400Mbps Interface

Each individual I/O on the two sides of the AccelArray platform contains a pre-diffused module (Figure 2). Each module includes a receiver, transmitter, clock generator, and variable delay line. The “transmit” and “receive” side meets the tight timing requirements of the DDR interface. The 16-bit wide core can be used in parallel to scale up to 32-bit, 64-bit, and higher bus widths, providing unlimited design flexibility.

The receiver module generates a 2X clock and delivers it to the serializer with minimum skew. The serializer performs parallel to serial conversion of data. The receiving clock has a 90-degree phase shift. The same clock is then sent to the core. The module also deserializes the data from outside.

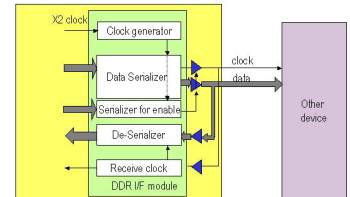


Figure 2 AccelArray DDR Macro

### DDR Interface Compiler Offers Great Flexibility and Ease of Use

AccelArray logical and physical compilers support all kinds of DDR interfaces in addition to SDR interfaces. The logical compiler generates a netlist based on the type of DDR selected by the user. The correct configuration of clock, address, control, DQ, DQS and command are all automatically executed. The physical compiler then generates the DDR I/O with well-controlled skew. The specific DDR width and bit selection is then implemented by customized metal layer options. ■