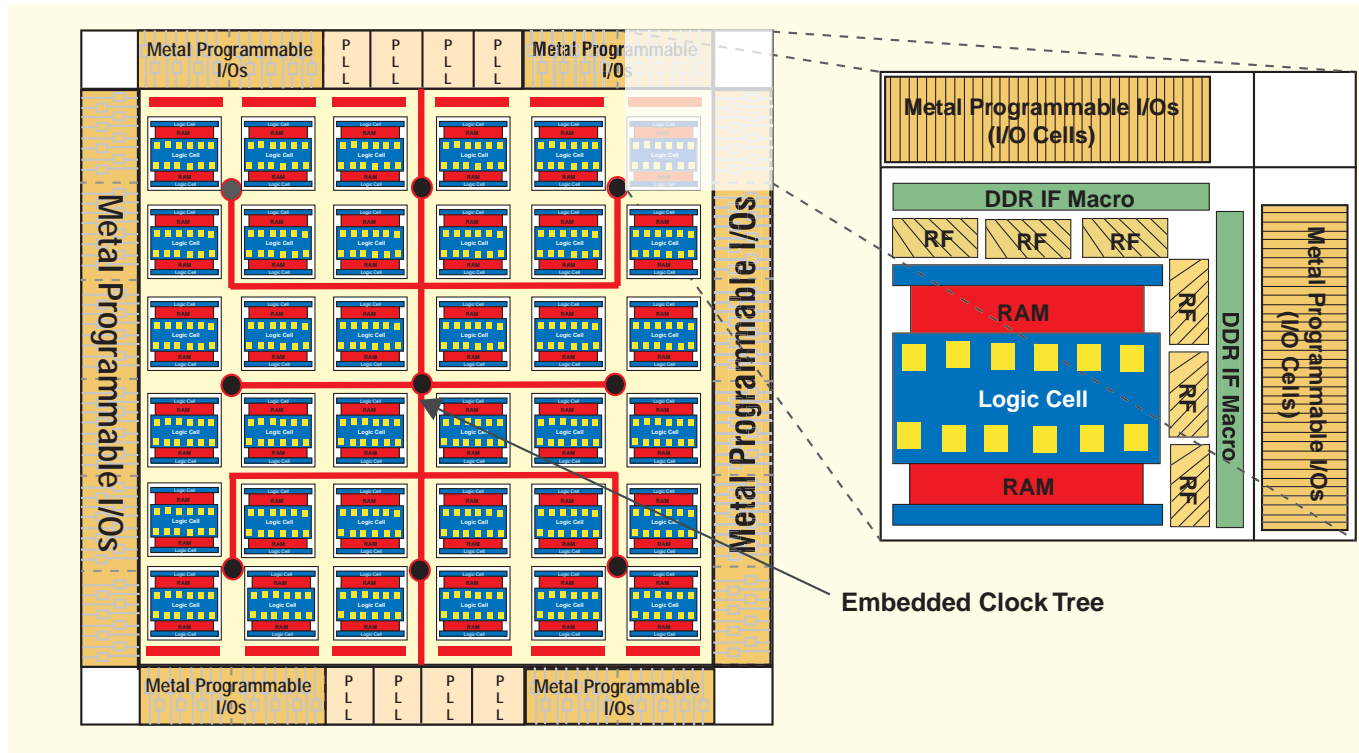


AccelArray™



Embedded Clock Tree

► Description

AccelArray™ is an innovative technology and design approach that leverages Fujitsu's ASIC design experience, system-level expertise and commitment to offer unprecedented performance with a short time to market. Additionally, AccelArray offers significantly lower up front NRE costs compared to cell-based ASICs in 0.11µm technology. The architecture eliminates many design tasks that consume a considerable amount of time in back-end physical design, such as DFT insertion,

power mesh and clock tree synthesis. In addition, internal timing closure, cross talk analysis and corrections, and I/O timing closure are extremely simplified.

AccelArray's unique architecture offers the lowest power solution in its class. Power dissipation is significantly improved, over similar solutions, through the use of embedded Flip Flops, pre-defined clock tree architecture and optimized libraries for gate density and lower power.

► Architecture

Architecture reduces tedious physical design tasks in 0.11µm

- Pre designed global clock trees

- Simplified timing closure with built in I/O interface
- Resolves signal integrity issues
- DFT free

► Features

- High performance and density
 - 333 MHz core system frequency
 - 800MHz analog PLL
 - Specifically designed libraries for high density and low power
- Fast time-to-market (TTM)
 - Development time
 - Re-spins
- Programmable embedded memory
 - Single and dual port memory at 333 MHz
 - Selectable bits and words
- Analog PLL
 - Up to 8 clock domains available
 - Input frequency: 25-800 MHz
 - VCO output frequency: 400-800 MHz
 - Output divider: 1,2,4,8,16
- Metal Programmable I/O technology
 - Fully configurable I/O core and I/O power supply pads
- Supports industry's widest range of I/O standards
 - HSTL, LVCMOS, PCML, LVDS (622 Mbps), SSTL-2, PCI-66, PCI-X
- Source synchronous interface support
 - DDR / DDRII-SDRAM, DDR / QDR / QDRII-SRAM, SDR, CAM
- Pre-defined test insertion
 - Logic SCAN / RAM BIST / JTAG / test bus (PLL) are provided
 - Customer's functional test vector is optional
- Platforms supports a variety of options
 - I/O Cell slots: 472 to 1128
 - Embedded memory: 860K to 4.6 Mbits SRAM
 - Available ASIC gate counts: 512K to 3842K
 - Embedded Flip Flops: 23K to 173K (additional to available gates)
- Packages
 - FCBGA: 625-1681

FUJITSU MICROELECTRONICS AMERICA, INC.

Corporate Headquarters
1250 East Arques Avenue, Sunnyvale, California 95088-3470
Tel: (800) 866-8608 Fax: (408) 737-5999
E-mail: inquiry@fma.fujitsu.com Web Site: <http://www.fma.fujitsu.com>