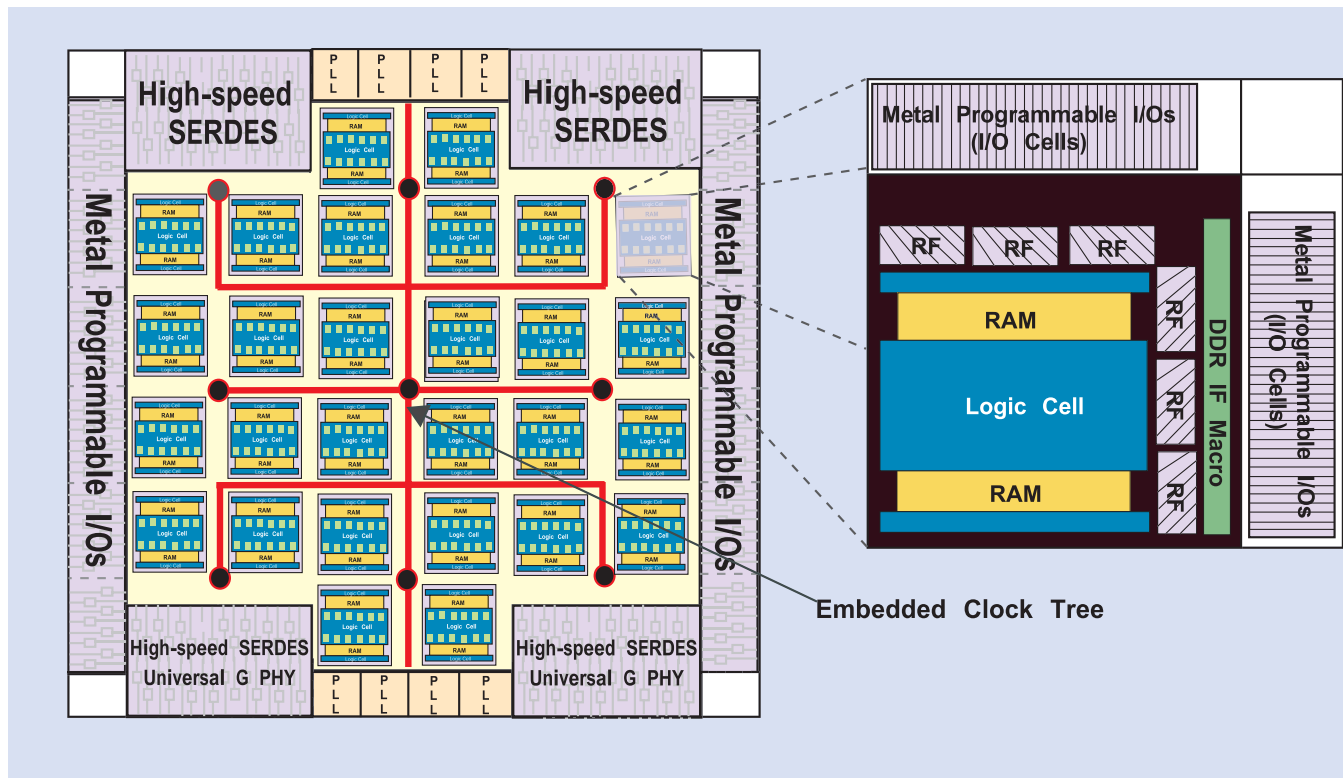


# AccelArray™ Giga Platforms



## Description

Giga platforms address the specific needs of mid-volume vertical markets that require the performance of cell-based ASICs. These platforms leverage Fujitsu's decades of ASIC design and system-level expertise in the networking, storage networking, next-generation consumer electronics and imaging markets.

Giga platforms reduce back-end physical design time such as DFT insertion, power mesh, clock tree synthesis and simultaneous switching output (SSO) analysis, all of which can consume a considerable amount of time. The giga

platform offers up to 150 Gbps of full-duplex SERDES aggregated bandwidth by incorporating pre-diffused universal G-PHY and S-PHY macro cells.

### Universal G-PHY

Based on proven XAUI technology, universal G-PHY is a multi-gigabit transceiver macro that performs high bandwidth data communication while consuming little power. G-PHY supports a multitude of standards including Serial Rapid I/O, Fibre Channel, SAS, SATA and PCI Express.

## Architecture

### Universal G-PHY Macro

- Flexible parallel transmitter and receiver
- Receiver with a common PLL (n=1~4)
- Programmable output level
- 1.8VPCML, LVDS, OIF/SxI-5
- Variable output current
- Pre-emphasis to compensate for skin effect and dielectric loss in backplane and/or cables

# AccelArray™ Giga Platforms

## ▶ Architecture

- Variable pre-emphasis current control
- On-chip termination resistor - 50/75ohm selectable receiver and PLL
- Wide range of operation frequencies
- 1GHz/1.25~1.56GHz selectable mode
- Clock Data Recovery (CDR)
- Dual loop PLL (analog loop + digital loop)

## ▶ Features

### Universal G-PHY

- 0.11µm CMOS process using 1.8V and 1.2V supply voltage
- Flexible array widths - macro is 4 channel, any channel can be turned off and on
- Multiple input/output data rates
- 0.78-0.5Gbps, 1.56G-1.0Gbps, 3.125G-2.0Gbps
- Dedicated CDR in each receiver channel
- Support for multiple standards, e.g., XAUI, Fibre Channel, SAS, SATA and PCI Express
- Wide range of reference clock frequencies possible

### Universal S-PHY

- SFI-4, SFI-4mod, HyperTransport, RapidIO, SPI4P2
- ~ 800Mbps, 16-bit data, SDR mode
- SPI4P2/NPSI
- ~ 1.3Gbps, 16-bit data + 1 control, DDR clock
- Dynamic alignment using DLL

	Voltage	Interface Type	Speed
<b>S-PHY</b>	1.2v/2.5v	SFI4	622M-800M
	1.2v/2.5v	Hyper Transport	400M, 600M, 800M
	1.2v/2.5v	RapidIO	500M, 700M
	1.2v/2.5v	SPI4P2	622M-800M
<b>G-PHY</b>	1.2v/2.5v	XAUI	3.125G
	1.2v/2.5v	FibreChannel	1.0G, 2.0G
	1.2v/2.5v	RapidIO	1.25G, 2.5G, 3.125G
	1.2v/2.5v	PCI express	2.5G
	1.2v/2.5v	CDR	622M-3.125G

## FUJITSU MICROELECTRONICS AMERICA, INC.

1250 E. Arques Avenue, Sunnyvale, CA 94088-3470  
 Tel: (800) 866-8608 Fax: (408) 737-5999  
 E-mail: inquiry@fma.fujitsu.com Web Site: <http://www.fma.fujitsu.com>

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