

AccelArray IP-Rich Platform for Optimized Functionality, Performance and Time to Market

Time-to-Market

AccelArray IP-rich platforms enable users to significantly improve their time-to-market and lower the total cost of ownership when designing complex, application-specific system-on-chip (SoC) products compared to conventional ASICs.

The total cost of ownership can be lowered due to reduced masks and design service costs, fewer IC designers allocated to the ASIC project, and reduced production lead time that can lower inventory costs.

IP-Rich Platform

Based on Fujitsu's rich set of IP libraries, AccelArray platforms consist of both functional and infrastructure IPs, as well as definitions and interfaces for higher layers of abstraction in the design process.

Functional IPs include microprocessor cores such as ARC and ARM, DSP macros, specific logic functions, memory, and interfaces such as PCIx, PCI Express or high-speed interfaces such as XAUI or Fibre Channel SERDES.

Infrastructure IPs include clock and power-mesh architectures, embedded I/O buffers, analog macros such as Phase Lock Loops (PLLs), cell libraries and test circuits.

Fujitsu's extensive IP libraries include pre-built, pre-verified macros in the AccelArray platforms. Built on 0.11-micron process technology, these platforms contain very specialized sets of soft and pre-diffused IPs that meet the needs of many market segments, such as networking, storage and medical imaging, where high bandwidth and high performance are required.

An integral part of Fujitsu's strategy of supporting SoC platforms for the communication market is the suite of high-speed macros that support chip-to-chip, board-to-board interfaces such as Rapid I/O, PCI Express, SPI4.2, SFI4, XAUI and Fibre Channel in AccelArray platforms. These platforms have been tested and verified for the worst-case signal integrity, simultaneous switching outputs (SSO) and IR drop issues.

These capabilities enable Fujitsu to offer a significant advantage to its

customers, enabling them to design SoCs on AccelArray platforms in as little as eight weeks while minimizing risk and reducing the total cost of ownership. For more information, see <http://www.fma.fujitsu.com/accel/>

Highly Reliable Nano-Clustering Silica with Low Dielectric Constant and High-Elastic Modulus for Copper Damascene Process

Engineering members from Fujitsu Limited Interconnect Technology Division have presented a paper related to the essential technology needed to bring the 65nm technology to the market in the first half of 2005. The paper was presented at the International Interconnect Technology Conference (IITC), which was sponsored by IEEE last June.

According to the paper, by controlling the size and distribution of pores in the NCS precursor, Fujitsu developed highly reliable nano-clustering silica (NCS) with low dielectric constant ($k < 2.3$) and high elastic modulus ($E = 10\text{Gpa}$) for copper damascene process. Using this material in a process compatible with the 90nm technology node, Fujitsu has successfully demonstrated Cu wiring in NCS dielectrics. For more information, see

<http://www.fma.fujitsu.com/wafer/>

