

AccelArray™ Technology

Innovative technology that addresses design challenges in 0.11µm technology with low non-recurring engineering costs and fast turn-around time

Over the last decade, standard-cell ASICs have been a preferred choice for many applications that place a high priority on lowest unit cost and highest performance objectives. Meanwhile, gate array technology has continued to support low- to mid-density applications with moderate performance, due to lower non-recurring engineering (NRE) costs and faster turn-around time (TAT) attributes.

As OEM customers focus more and more on cost reduction, ROI, and time-to-market criteria, developing an ASIC has become a decision with a much larger impact. In addition, as the technology roadmap moves down to deeper sub-micron levels, such as 0.11µm and 90nm processes, an exponential increase in mask cost contributes heavily to the upfront

NRE cost. Another inherent problem with deep sub-micron technology is the increased complexity of the back-end ASIC design. All these factors fueled the need for Fujitsu to develop an innovative solution that addresses design challenges in 0.11µm technology of offering a low-risk, fast turn-around time, and yet low NRE cost solution.

AccelArray Offers Flexibility and Performance

This new technology, with its innovative architecture, addresses the design challenges in 0.11µm technology by offering a high-performance customized solution combined with a fast turn-around time and low NRE cost. The AccelArray has created a very impressive alternative to the 0.11µm standard-cell ASICs. Fujitsu now can

deliver to the customer the ultimate flexibility and performance with several base frames of complex logic cells, embedded flip flops, configurable embedded memory, programmable I/Os that support many kinds of I/Os including LVDS and LVCOMS, and a highly automated methodology in test insertion.

Architecture Addresses Key 0.11µm Technology Design Issues

There are fundamental challenges in deep sub-micron designs. The increasing effect of capacitive coupling between signals (crosstalk) has a negative impact on signal integrity. AccelArray architecture addresses signal and power issues, such as IR drop and Xtalk, which produces more predictable and repeatable design closure.

