Semiconductor Integration Considerations for Broadband Wireless Access (BWA)

Technical challenges & architectural requirements

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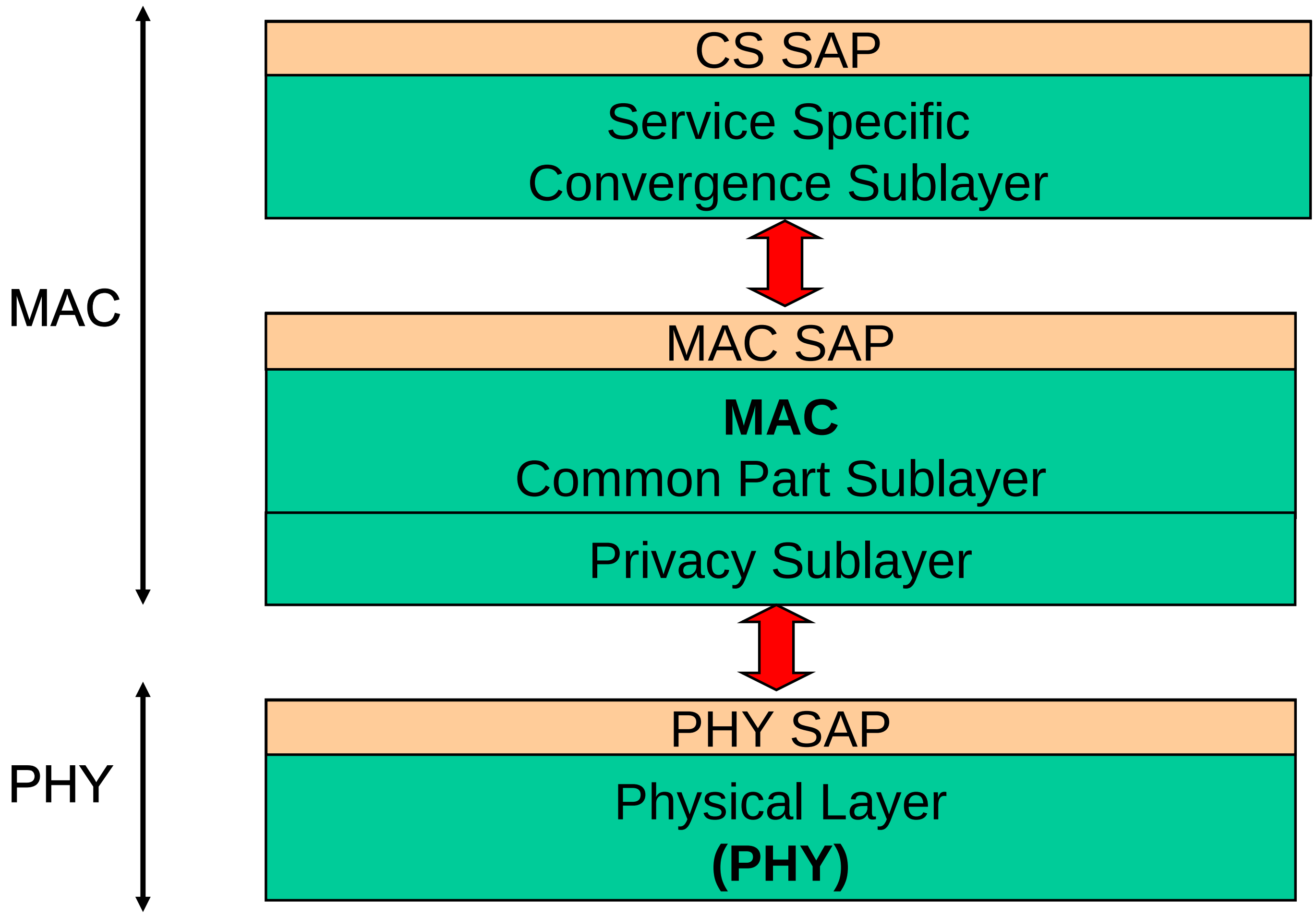
Contents

802.16 BWA Overview

- **Standard for wireless metropolitan area networks (WirelessMAN™)**
- **Supports a variety of services such as IP, voice over IP, and streaming video**
- **Protocol independent supporting ATM & packet based protocols**
- **Point-to-multipoint broadband wireless access**
- **Adopted to address:**
  - Operation in 2-11 GHz spectrum
  - Eliminates need for directional LOS propagation
  - Greater range & high data rates
- **Supports Multiple services simultaneously, with different *QoS* priorities**

802.16 Reference Model



PHY Design Challenges (1)

- **Standards compliance**
  - IEEE 802.16-2004 OFDM-256 standard
  - Interoperability trials through WiMAX
- **Design Complexity**
  - Larger FFT size i.e 256 points or more
  - Flexible modes of operation i.e channel bandwidths, cyclic prefix lengths, frame sizes, etc
  - Complicated Forward Error Correction – Reed Solomon + Viterbi decoding
  - Requirement for Full Duplex Operation
  - Addition of subchannel modes for multi-user operation
  - Adaptive modulation and coding
  - Stringent system margin requirements for modem
- **Non-Line-of-Sight (NLOS) performance**
  - Operate over large distances in NLOS environments with significant multi-path
- **Programmable Header & MAP decoding using an integrated Lower MAC Processor**
  - Programmability ensures future standards compliance
- **Area and power optimized design**

PHY Design Challenges (2)

- **Support for:**
  - WiMAX™and other specified channel bandwidths from 1.25 to 20 MHz
  - Frame sizes ranging from 2.5 to 20 ms
  - Guard Intervals of 1/4, 1/8, 1/16 or 1/3
  - BPSK to QAM-64 modulation types across all channel bandwidths
  - Supports the maximum 73 Mbps data rate
  - Base Station (BS) and Subscriber Station (SS) Operation
  - Low latency design
  - Excellent system margin and performance in the presence of fading channels
- **Time-Division Duplex (TDD)**
  - DL & UL time-share the same RF channel
  - Dynamic asymmetry
- **Frequency-Division Duplex (FDD)**
  - Downlink & Uplink on separate RF channels
  - Static asymmetry
  - Half-duplex SSs supported
  - Full-duplex BSs supported

Complexity of MAC Design

- **802.16 MAC involves complex software design with many challenges:**
  - Efficient use of RF spectrum
  - Very high bit rates, downlink and uplink
  - Hundreds of connections and users
  - Routine tasks such as data encryption/decryption, CRC checking/appending, etc. take up significant portion of the CPU bandwidth, leaving less room for more complex tasks
  - QoS requirements
  - Enhanced Security and Privacy
  - Provide convergence layers to various protocols, e.g. ATM, IP, Ethernet, …

MAC Partitioning

MAC design and implementation can be divided into 2 Modules:

Upper Layer MAC Software (UMAC)

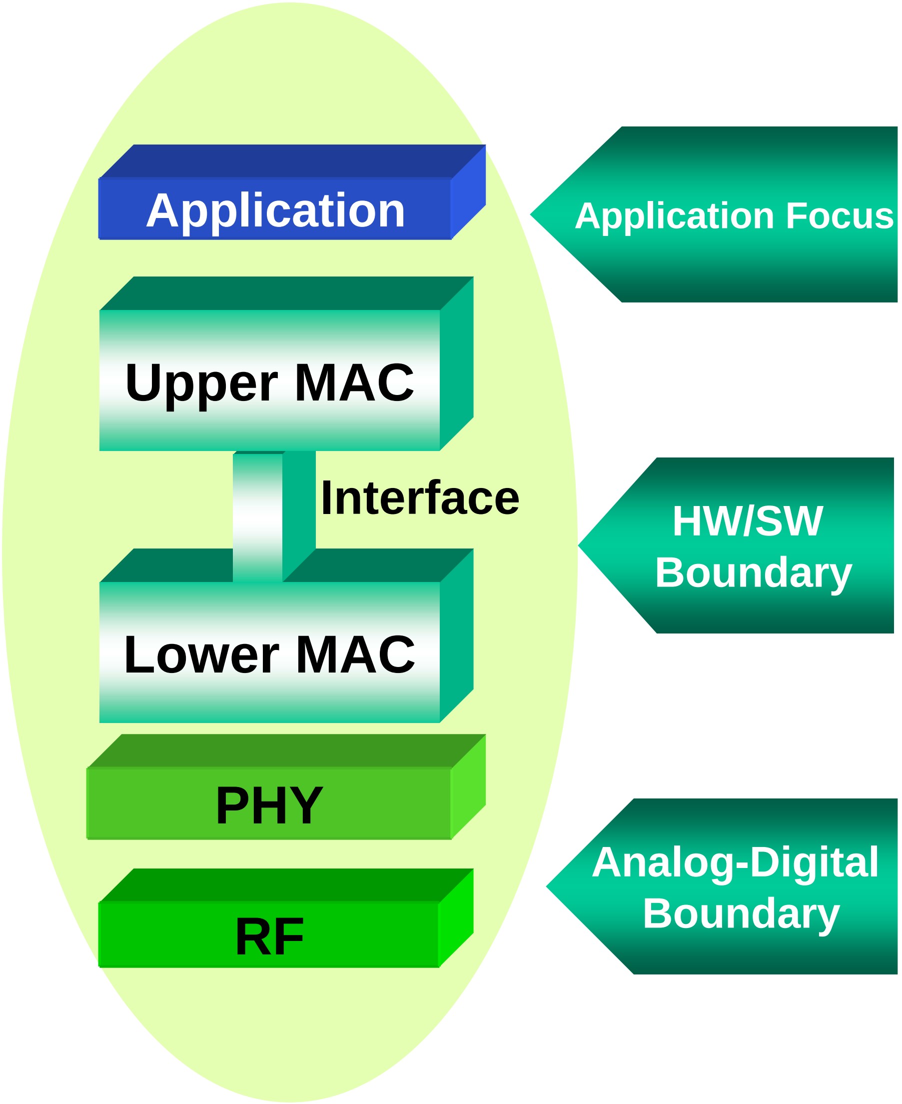
- **Implemented on either internal or external Network Processor**
- **Provides higher level 802.16 MAC functionality**
  - MAC Management
  - Service specific convergence sublayers
  - Common Part Sublayer
  - Key management
- **Different versions for BS and SS**
- **BS version is likely to run on a more powerful processor**

Lower Layer MAC Software (LMAC)

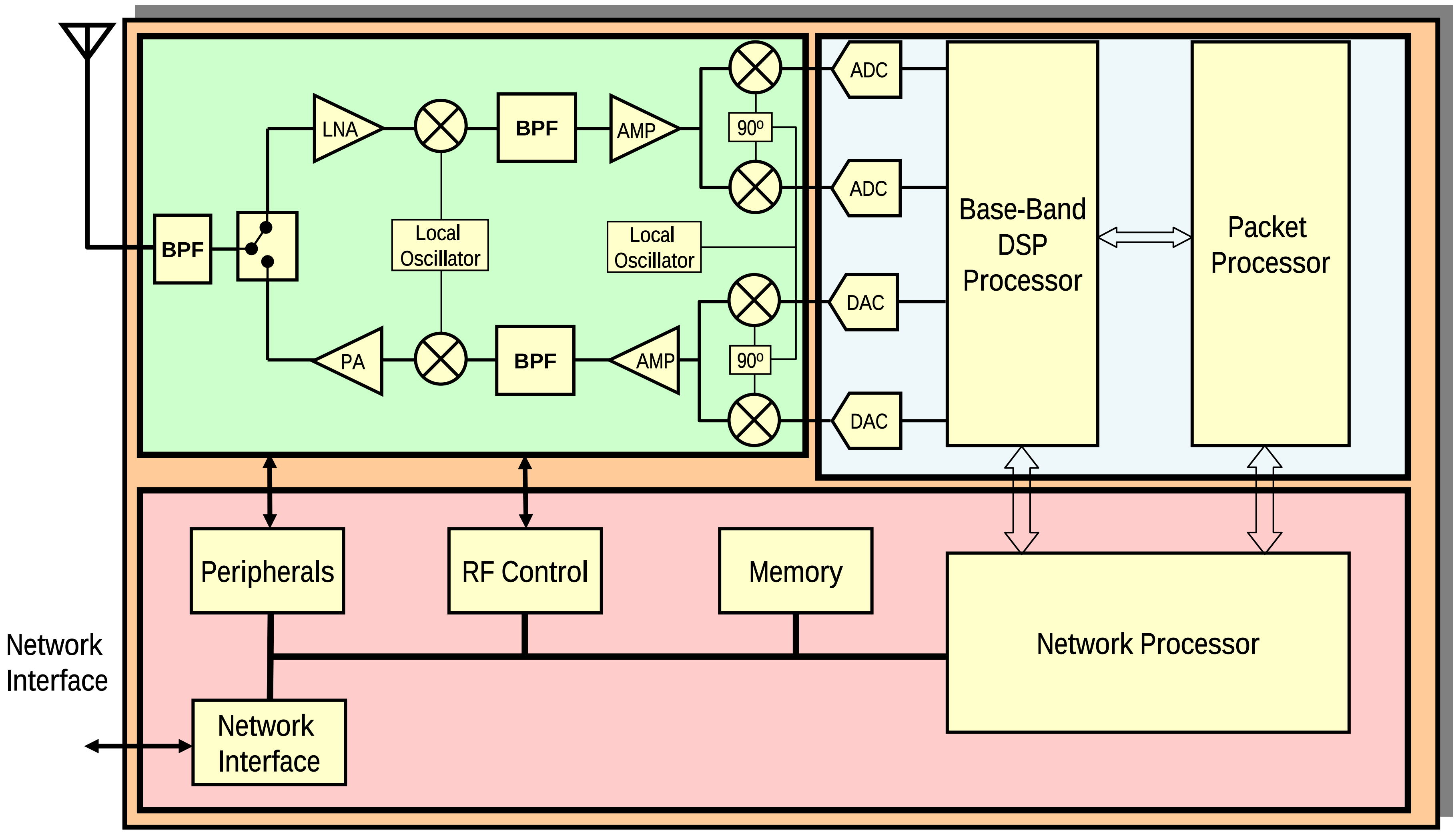
- **Bridge between UMAC and the PHY**
- **Isolates PHY complexity from UMAC**
- **Programmable = Flexible solution**
- **Off-loads some of the burden from UMAC by performing:**
  - Data Encryption and Decryption
  - CRC and HCS generation / checking
  - CID based filtering
  - Transmission Convergence Sublayer
  - PDU classification and FEC block processing
  - Provides PHY access primitives
- **Different versions for BS and SS**

MAC Design Challenges

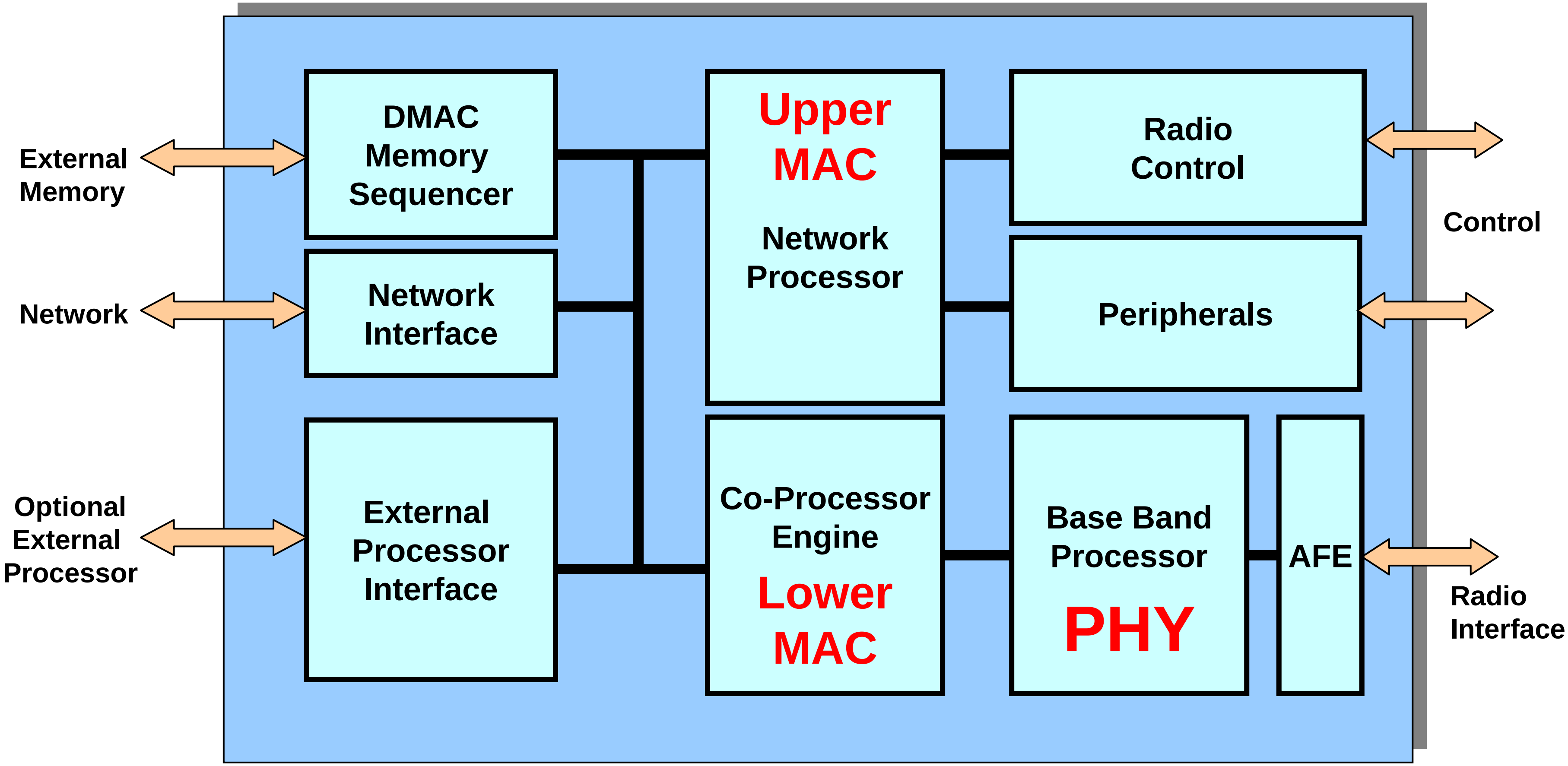
- **How is Upper and Lower MACs interfaced with each other?**
  - **Data transfer**
  - **Flow control**
  - **Error handling**
- **Is the logical division of tasks between Upper and Lower MAC align with the capabilities of individual processors ?**
- **Do Upper and Lower MACs operate independently with *minimum possible interaction?***
- **Is resultant software architecture *inline with SoC architecture?***



Typical System Implementation



System On Chip Implementation

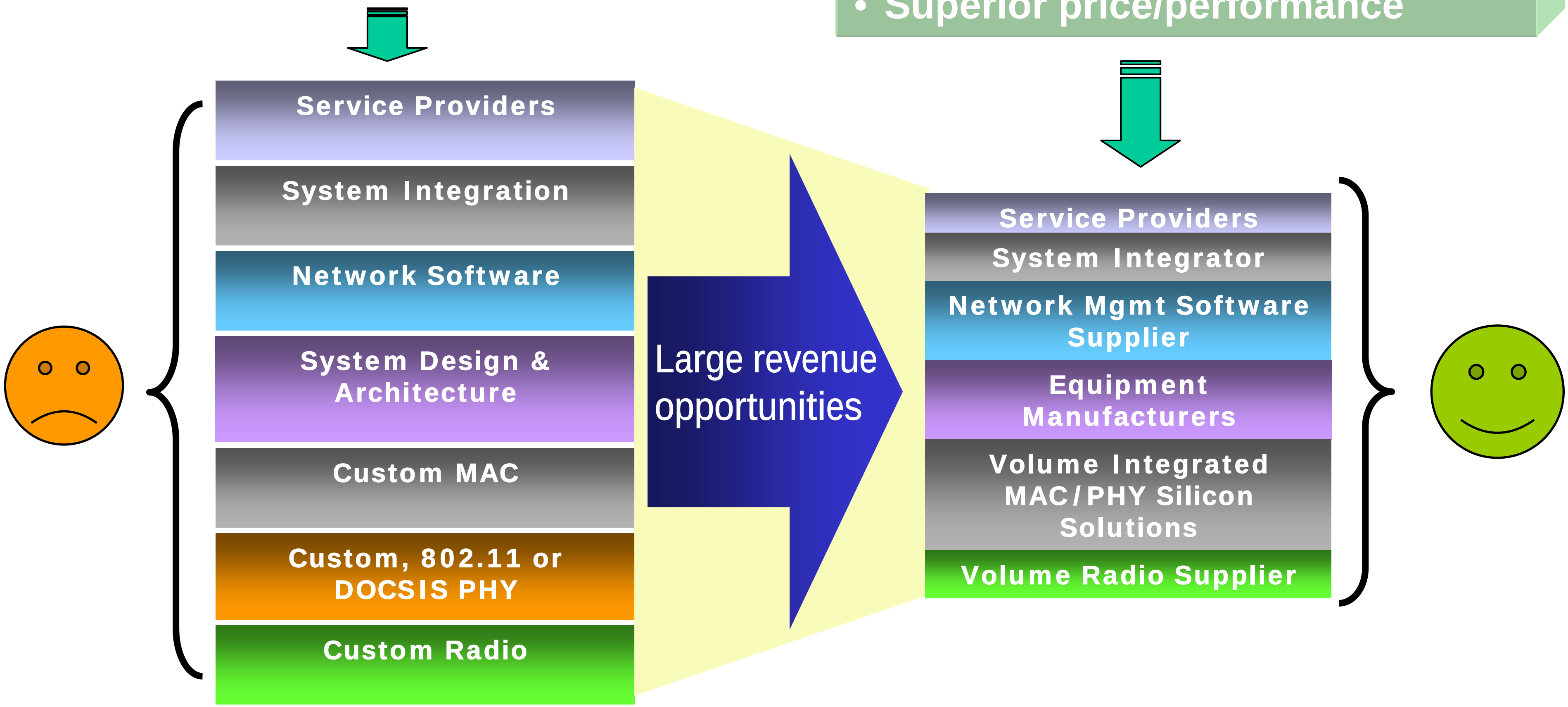


SoC

Volume Economics

Pre-Standard: Discrete Components
- Proprietary, vertical solutions
- No volume silicon market

Post-Standard: Integrated Solution
- Equipment interoperability
- Economies of scale
- Superior price/performance



FUJITSU

THE POSSIBILITIES ARE INFINITE