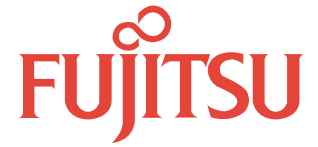
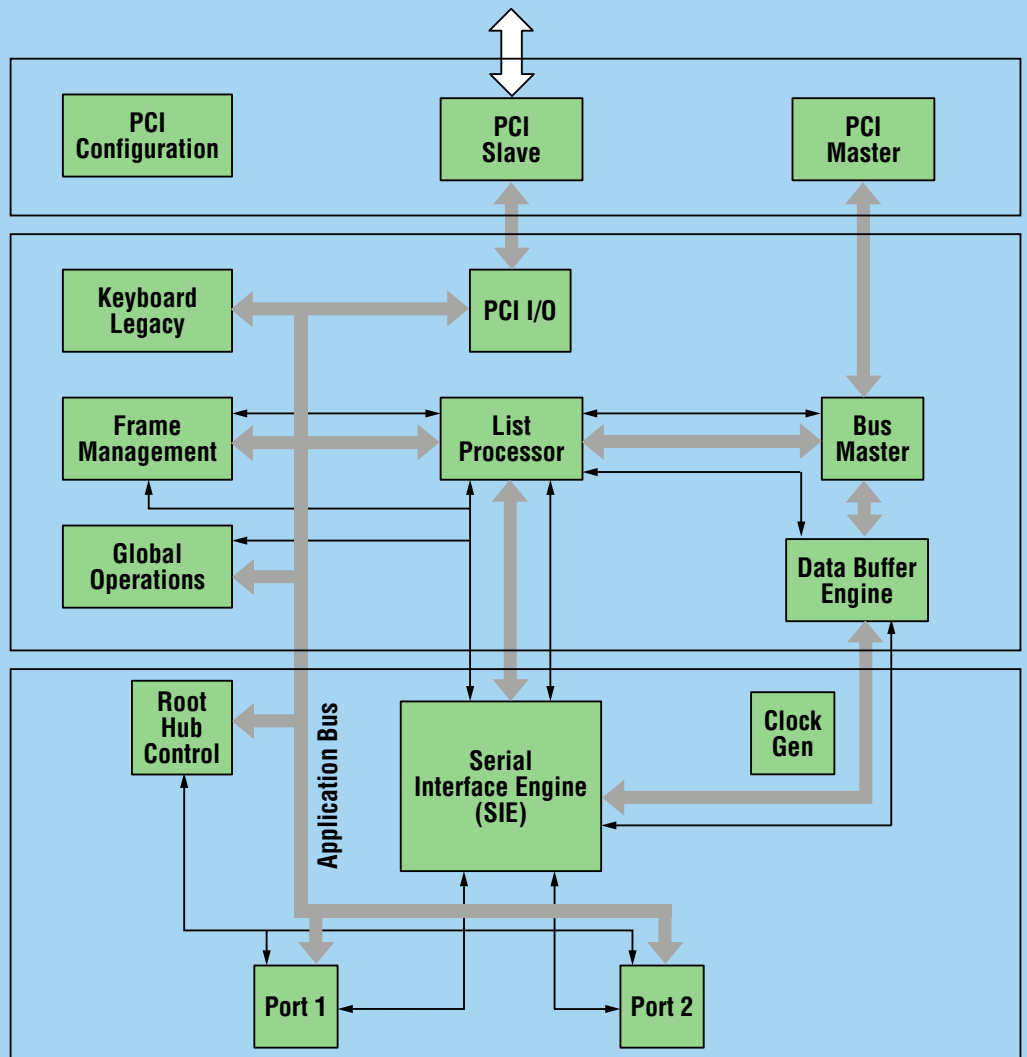


USB Host Controller Core



Core Block Diagram



► Features

- USB V1.0 compliant
- Open HCI V1.0 compliant
- 33 MHz PCI V2.1 compliant

- 12 Mb/s or 1.5 Mb/s data transfer rate
- Integrated root hub

► Benefits

- Soft core that can be implemented in any technology
- Silicon-proven to reduce time-to-market
- Legacy keyboard and mouse support

- Supports control, bulk, isochronous, and interrupt data transfer types to support various applications

USB Host Controller Core

► Description

The USB Host Controller is a synthesizable core and is part of the Fujitsu IPWare™ Library.

The core has a complete PCI to USB interface. It is fully compliant with USB specification 1.0 and the USB Open HCI specification authored by Microsoft, Compaq, and National Semiconductor. On the PCI side, it is compliant with PCI V2.1. The core can be used on a PC motherboard with a PCI bus or a stand-alone PCI-based ASSP.

The USB interface contains two primary modules. One is the serial interface engine (SEI), responsible for the bus protocol, and the other is the root hub, used to expand the number of USB ports.

The USB Host Controller incorporates much of the intelligence required for processing incoming and outgoing data, as well as legacy keyboard support for PS/2 keyboards connected to PS/2 keyboard controllers through Port 60/64.

This core is ideally suited for a variety of applications ranging from palmtop computing, mobile computing, and other consumer-related applications such as medical monitoring devices.

► Deliverables

A Fujitsu Microelectronics, Inc. application engineer works with the customer to select the process technology best suited to meet the customer's specific needs. After the technology is selected, the following information can be supplied to the customer:

- Encrypted Verilog RTL source code
- A hierarchical gate level netlist of the USB core

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