



Prism Circuits, Inc.

Multi Data Rate SerDes

Overview

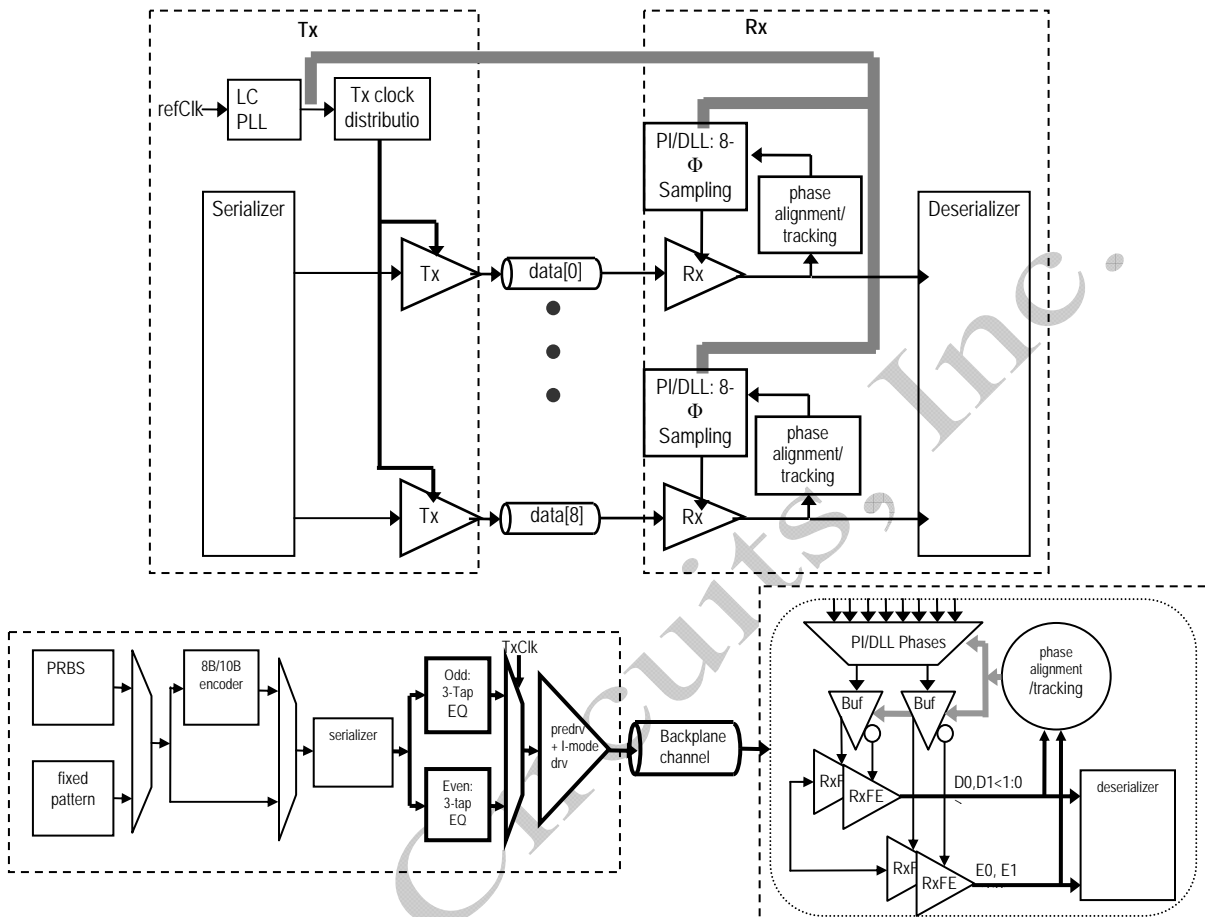
Prism Circuit's SerDes is optimized for high bandwidth (10G) backplane applications, while also enabling lower data-rate protocols like XAUI, SATA, PCIe Gen1 and PCIe Gen2. It consists of a custom circuit hard macro and a synthesizable soft macro for lower frequency logic. The hard macro is expandable to 8 transmit and 8 receive lanes. Each lane supports data rates up to 10 Gbps, enabling an aggregate bandwidth up to 160Gbps running full-duplex when all lanes are enabled. Lanes can be individually disabled for power saving configurations. Each hard macro has a PLL and clock distribution network that serves all 8 lanes.

The synthesizer can be driven by reference clock frequencies from 100 to 156.25 MHz. The TX has programmable 3-tap pre-emphasis to reduce pre-cursor ISI. To cancel ISI across difficult backplane channels, an adaptive decision feedback equalizer (DFE) is incorporated in the receiver. The I/O has low capacitance on-die termination to preserve signal integrity. Ample test features including BIST, BSCAN and Eye scan have been integrated to facilitate system bring up, as well as to enable HVM testing.

Features

- Fujitsu 65nm HP process
- Low area : 3.72mm² per Octal
- Low power consumption : 1.25W per Octal @10Gbps
- Multiple data rate support from 3.125Gb/s to 10.3125 Gb/s data per lane
- Low jitter LC-PLL supports up to 8TX and 8RX unidirectional lanes
- Per lane 3 Tap TX Pre-emphasis
- Amplitude control in TX
- Adaptive DFE in RX
- Per lane Clock/data recovery scheme
- Low latency TX & RX paths (TX: 25UI & RX: 50UI without coding scheme)
- Multiple power-saving modes
- Built-In-Self-Test features

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Views

- Verilog
- CDL Netlist
- Timing Views (.lib)
- ATPG models (Fastscan)
- GDSII
- Encrypted Spice Netlist

Integration & Documentation

- Datasheet and Specifications
- Application Notes
- ASIC/SOC Integration Notes

For more information:

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