

130nm node CMOS Process (CS90A)

Features

- **1-Poly and 8-Metal (7-Cu + 1-Al) Process**
- **Retrograde Twin Wells on P Epitaxial Substrate**
- **STI (Shallow Trench Isolation)**
- **Salicided Gate, Source and Drain**
- **Advanced Cu + Low-k Interconnects**

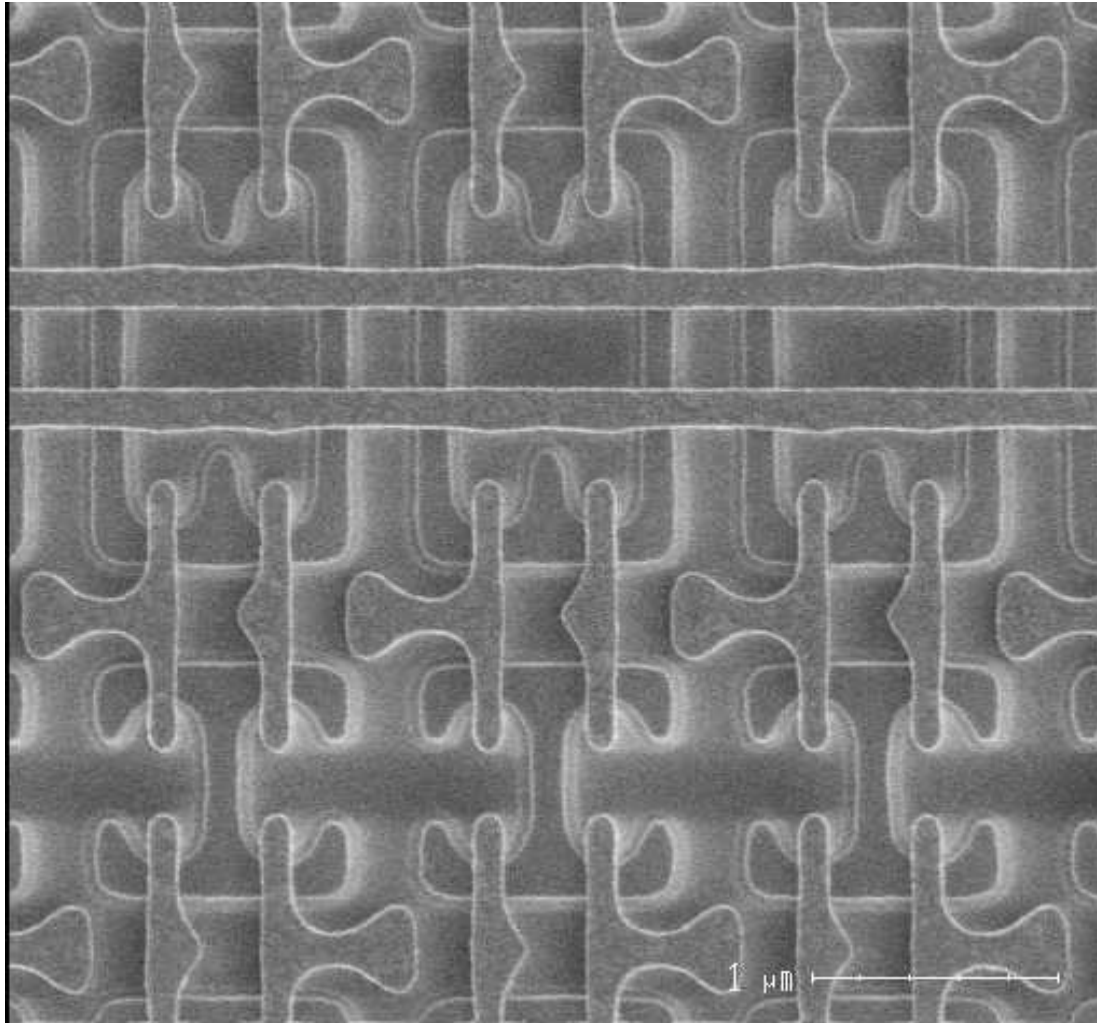
CS90A MOSFET Performance

THE POSSIBILITIES ARE INFINITE



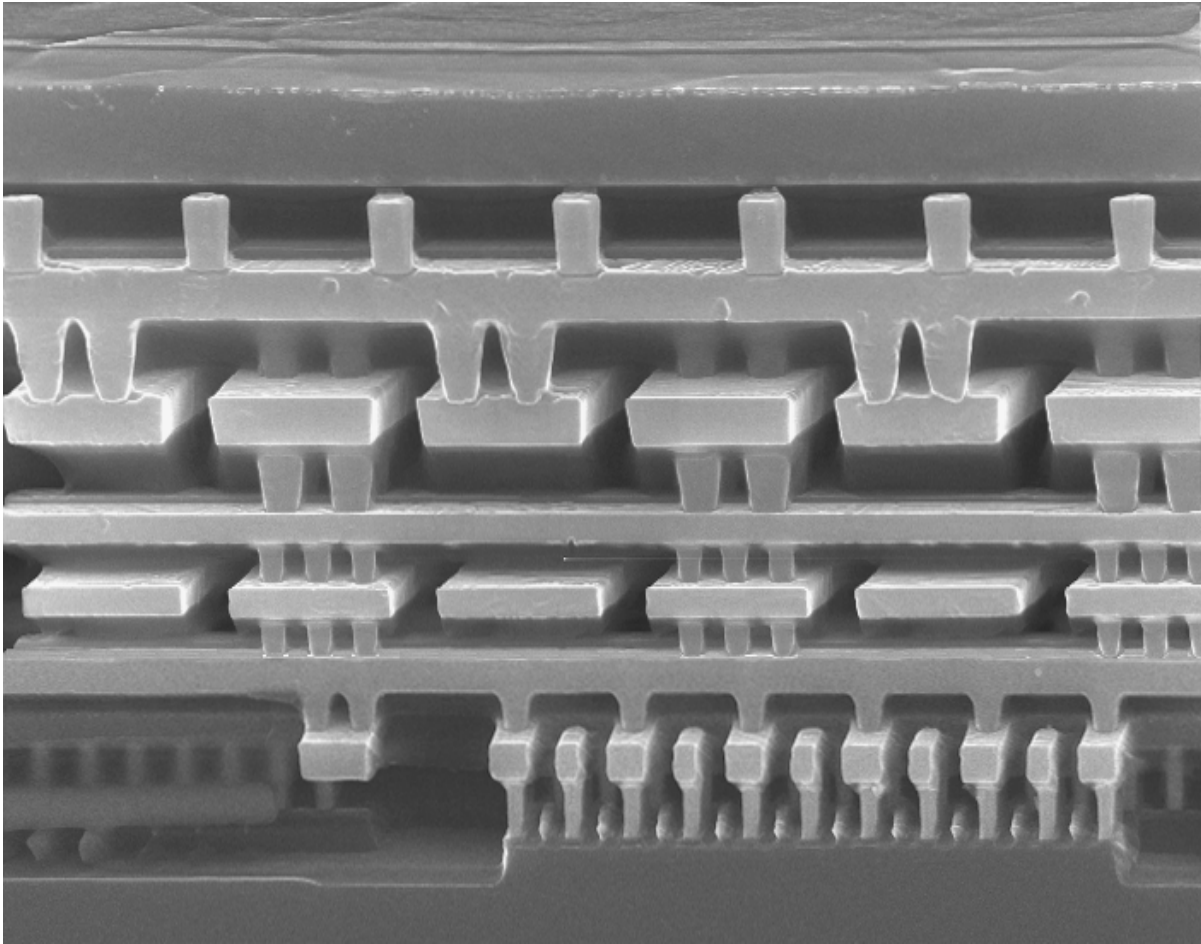
	UHS	HS	ST	LL
Gate Length	110 nm			
Gate Oxide	2.9 nm			
Supply Voltage	1.2 V			
nMOS I_{Dsat}	780 $\mu\text{A}/\mu\text{m}$	678 $\mu\text{A}/\mu\text{m}$	570 $\mu\text{A}/\mu\text{m}$	390 $\mu\text{A}/\mu\text{m}$
pMOS I_{Dsat}	-321 $\mu\text{A}/\mu\text{m}$	-276 $\mu\text{A}/\mu\text{m}$	-218 $\mu\text{A}/\mu\text{m}$	-150 $\mu\text{A}/\mu\text{m}$
nMOS I_G	10 pA/ μm			
pMOS I_G	-10 pA/ μm			
Gate Delay	14 ps	17 ps	28 ps	45 ps

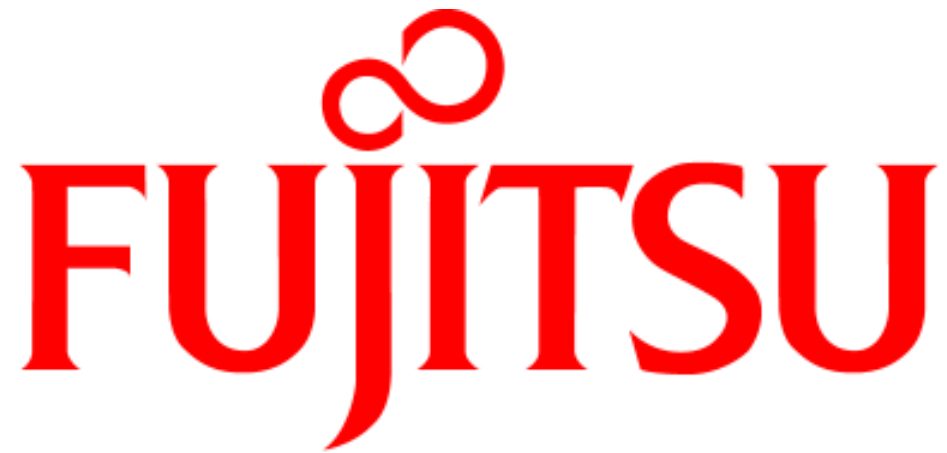
6T-SRAM



1.98 μm^2

Advanced Cu + low-k





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