

0.18 μ m node CMOS Process (CS80B)

Feature

- **2-Poly and 6-Metal Process**
- **Retrograde Twin Wells on P Epitaxial Substrate**
- **STI (Shallow Trench Isolation)**
- **Salicided Gate, Source and Drain**
- **CMP Planarized Interlevel Metal Dielectric**

Design Rules

Layer	Width (μm)	Space (μm)
Diffusion	0.22	0.24
Poly	0.18	0.24
Contact	0.22	0.26
Metal 1 - 4	0.24	0.24
Via 1 - 4	0.22	0.26
Metal 4 - 6	0.44	0.46
Via 4 and 5	0.44	0.46

MOSFET Performance

THE POSSIBILITIES ARE INFINITE



Supply Voltage	1.8 (3.3) V
Gate Oxide	4 nm

	nMOS	pMOS
V _{th}	0.53 V	-0.48 V
I _{Dsat}	0.56 mA/ μ m	-0.24 mA / μ m

Mixed Signal Options

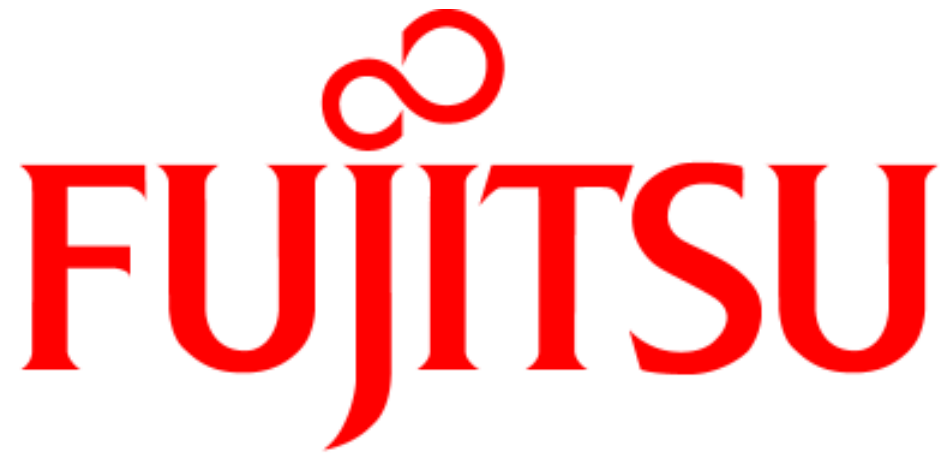
<p>Diffusion Resistor</p>	<p>1.6 kΩ /sq</p>
<p>Poly – Bulk Capacitor</p>	<p>2.47 fF/μm²</p>
<p>Poly – Poly Capacitor</p>	<p>1.38 fF/μm²</p>
<p>Triple Well</p>	<p>Available</p>

Circuit Performance

	Transistor	Gate
Density	148 K/mm ²	110 K/mm ²

	Inverter	2-NAND
Gate Delay	24 ps	39

	Cell Size	Speed
SRAM	4.9 /μm ²	1.3 ns



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