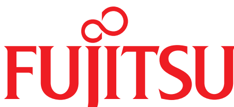


ASIC Packaging

Overview

Fujitsu, a world leader in packaging and interconnect technology, offers a full range of packages from the Quad Flat Pack (QFP) to Ball Grid Arrays (BGA) including Flip-Chip technologies. Fujitsu owns and operates package assembly integrated manufacturing facilities in Japan, shipping millions of packages per month for a wide range of applications.

For its ASIC customers, Fujitsu offers "one-stop shopping" for all their packaging needs. Fujitsu offers complete in-house, turnkey package design, as well as assembly and test services. All Fujitsu packaging solutions are RoHS compliant.

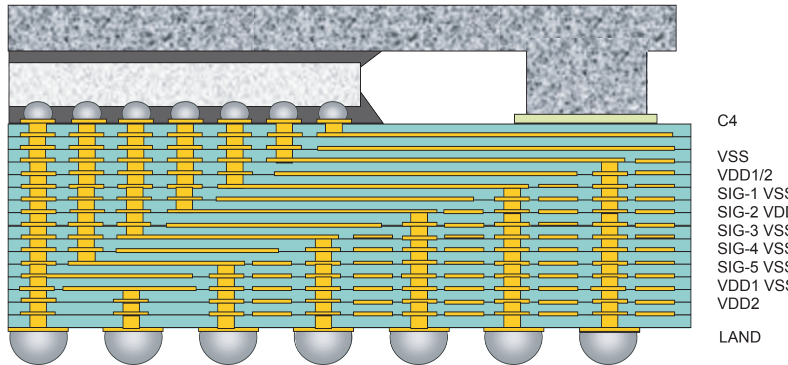
Package	Structure	Pin Counts	Clock Frequency	Thermal Resistance	Application
FC-BGA		450 to 2116	~10GHz	9°C/W (0m/s)	Internet router Server Workstation Public Transmission
FC-PBGA		450 to 2116	~5.0GHz	9°C/W (0m/s)	
TEBGA		256 to 1156	~300MHz	15°C/W (0m/s)	Internet Router PC Graphics
PBGA		256 to 1156	~300MHz	20°C/W (0m/s)	Internet Router PC Graphics
FBGA		64 to 584	~500MHz	25°C/W (0m/s)	PC Cellular phones DVC DSC
BCC		16 to 196	~5.0MHz	30°C/W (0m/s)	Cellular Phones DVC DSC
Stacking		Custom	Custom	Custom	Cellular Phones DVC DSC
PoP		Custom	Custom	Custom	Cellular Phones DVC DSC

ASIC Packaging

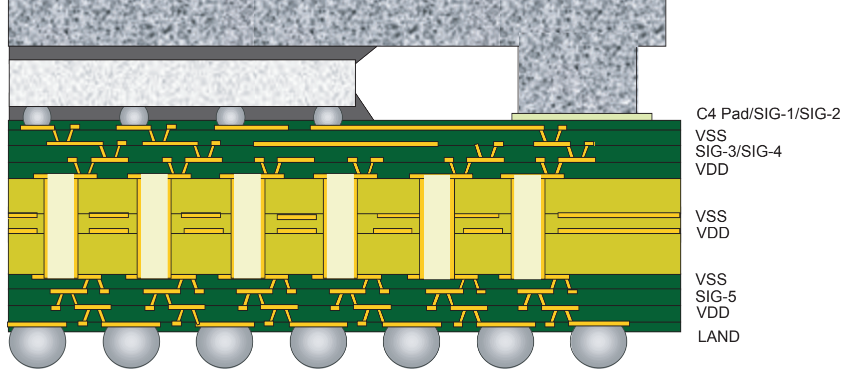
Offerings

- Flip-chip Ball Grid Arrays (FC-BGA) – combining high pin count, high speeds and signal integrity
- Thermal Enhance Ball Grid Arrays (TEBGA) – for high power devices.
- Fine-pitch Ball Grid Arrays (FBGA) – Providing small form-factor solution for portable devices

Traditional wire-bonded packaging no longer meets the requirements of today's high pin count and high speeds, such as those required in GHz-range sustained frequencies. As a result, the more sophisticated bumped-area flip-chip interconnect technology is preferred, due to the excellent thermal dissipation capability that is inherent in its structure. Inside its flip-chip BGA packages, Fujitsu's unique wiring strip interconnect technology has further enhanced the thermal and electrical characteristics of these packages.



Cross-Section Diagram of High CTE Ceramic FC-BGA



Cross-Section Diagram Build Up FC-BGA

ASIC Packaging

Key Features

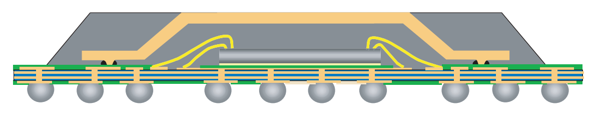
FC-BGA

- Glass ceramics or organic (build-up) substrate
- High pin-count – up to 2116 pins in 1.00mm ball-pitch, solid planes and stacked vias
- Some offered in 1.27mm ball pitch.
- Excellent electrical properties – low dielectric constant and inductance in multi-layer (10 or 19 layers) build-up and glass ceramic substrate technology
- Superb power dissipation – further augmented by the use of thermal compounds, heat spreaders or heat sinks
- Low profile JEDEC-standard packages – easily surface mountable on conventional standard PC boards
- Fujitsu's FC-BGAs are especially suited for highly integrated computing and communication applications
- Ultra-thin profile, including heat spreaders (2.5mm to 3mm)
- Moisture resistant (JEDEC Level 3)

TEBGA

Standard Features

- Thermal-efficient integrated heat spreader for high-power design applications
- 1.27mm and 1.00mm ball pitch
- Surface mountable and JEDEC compliant
- TEBGA has approximately 20% better thermal performance over standard PBGA
- Reliable Over Molded Package

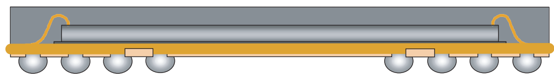


TEBGA Cross-Section

FBGA

Fine-pitch BGA (FBGA) technology, one of Fujitsu's near Chip Scale Packaging (CSP) solutions, provides the benefits of reduced package space and weight. FBGAs are available in rectangular and square body size packages.

- Can be low pin count packages – some as low as 32 pins and as high as 496 pins with 1.2mm height.
- JEDEC Standard fine Ball pitch from 0.5mm to 0.8mm
- Small-outline and Low-profile package
- Provides cost-effective packaging density
- Good for today's demanding portable applications

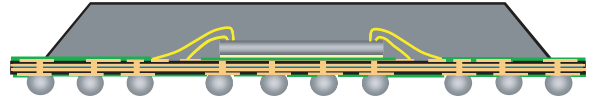


FBGA Cross-Section

PBGA

Plastic BGA is an Over Molded Pad Array Carrier (OMPAC) style package designed for low-cost applications. This BGA utilizes a four-layer printed circuit board substrate that provides a high level of electrical performance. PBGA packages provide good thermal performance with moderate power dissipation. Thermal performance can be further enhanced through the use of additional thermal balls placed directly under the die mounting area. Epoxy-filled through holes in the substrate ensure a high level of reliability. For very cost-sensitive designs, a lower performance, two-layer, low-cost printed circuit board version of PBGA is also available.

- 1.27mm and 1.0mm ball pitch
- Square body
- Pin-count: 256–868 pins



PBGA Cross-Section

ASIC Packaging

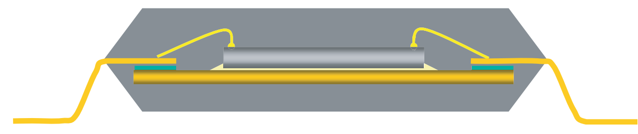
Key Features (Continued)

QFP

Fujitsu offers QFP packages in 0.80, 0.65, 0.50 and 0.40 lead pitches. The leads of the package, which extend out from four sides, are either gullwing (L-shaped) or straight. These packages conform to industry standards with pin counts ranging from 32 to 368 pins. Lead frames are constructed with either iron/nickel alloy or copper alloy that offers good thermal and electrical performance.

The Heat-spread QFP (HQFP) package uses a heat-spreader that is attached to the bottom of the die integrated to the lead-frame. HQFP offers better thermal performance than traditional QFP packages.

For ASIC applications, two additional types of QFP packages, the Low-profile QFP (LQFP) and Thin QFP (TQFP), are available. The mounting height of the TQFP packages is the thinnest with a maximum height of only 1.0mm. The LQFP packages have a smaller body size than the regular QFP. The lead pitch in both LQFP and TQFP packages is 0.40mm and 0.50mm.



QFP Cross-Section

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