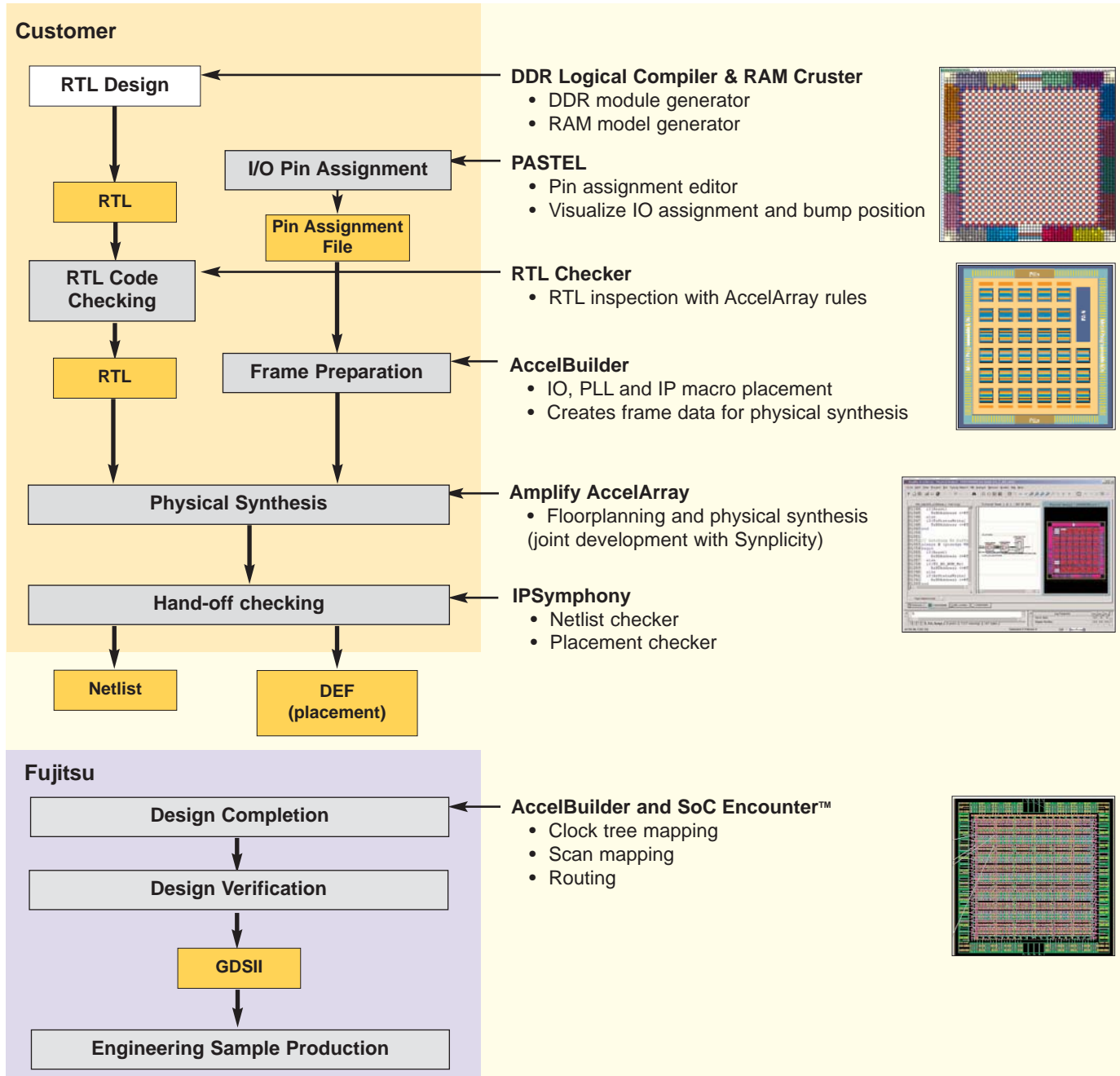


# AccelArray™ Tools & Methodology



▶ **Description**

Fujitsu's AccelArray methodology provides an easy-to-use tool set specifically designed to reduce some of the most tedious design tasks through the design process and onto the final

placed netlist handoff. The optimized methodology enables Fujitsu to tape out and fabricate designs in a fraction of the time needed for a traditional ASIC.

# AccelArray™ Tools & Methodology

## ▶ Features

The AccelArray design tools are available to Fujitsu's customers as a part of comprehensive AccelArray tool and methodology package. Included in the front-end package is the following set of advanced tools:

### **PASTEL**

Used for generating the I/O pin assignment, this tool provides a graphical environment for assigning pins and I/O pads, viewing the chip and package, and checking the final pin assignment. Using templates prepared for each frame and package combination, the user can assign pins via the GUI or provide a CSV file as input.

### **DDR Logical Compiler**

This easy-to-use tool greatly simplifies the design and support of DDR interfaces up to 400 Mbps. The logical compiler (LDDR) generates a DDR-I/F module (Verilog-HDL netlist) that guarantees post-layout timing operation, based on the user's configuration and requirements. The DDR-I/F module is later mapped to the dedicated DDR-I/F macro cells provided in the AccelArray frame, by use of the Physical DDR compiler tool (PDDR).

### **RAM Cruster**

This tool creates the RAM models for the specific bit/word combinations that are used in the design. These are based on the

RAM resources available on each AccelArray frame. The models are generated as Verilog-HDL cell based Netlists.

### **Accelbuilder**

Used to generate the design-specific frame, this tool automatically places the I/O cells based on the PASTEL pin assignment and maps the PLL and DDR macro cells to the available resources on the frame master. The resulting data is used as input to drive the physical synthesis.

### **Amplify® AccelArray**

Jointly developed with Synplicity, this physical-synthesis tool is used exclusively with AccelArray, providing automatic RAM placement, floorplanning and physical synthesis based on the chosen AccelArray frame. Cross-probing between RTL, netlist and placement views is available to improve the debugging process.

### **IPSymphony™ (Hand-off/Release Checker)**

IPSymphony is used to check whether or not a customer's netlist and placement data (DEF) satisfies Fujitsu's hand-off/release criteria. This tool verifies the final netlist and database, and generates all outputs necessary for handoff to Fujitsu for layout completion and manufacture. Handoff iterations are avoided because physical issues are addressed in the front-end design process.

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