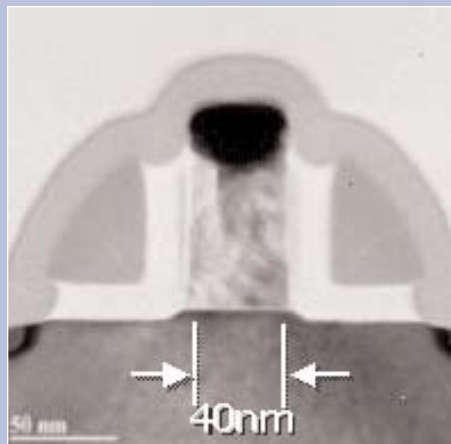


90nm CMOS Standard Cell

CS101 ASIC Series

High-performance transistors

- Advanced lithography and etch technology to achieve 40nm gate length
- Low temperature process for shallow junction
- Process optimization for high carrier mobility



40nm gate for 90nm node



9Cu/1Al interconnect

Features

- High integration
 - Transistor of 80nm gate length (ITRS road map 90nm)
 - 10-layer fine pitch, copper wiring, and low-k insulating material techniques
 - Maximum 91 million gates (nearly twice that of 0.11μm technology)
- Low power consumption/low leakage current
- I/O with pad structure with fine pad pitch technology for chip size reduction
- High-speed library and low-power library available
 - Ultra high speed: CS101HU
 - High speed: CS101HZ, CS101MZ, CS101SZ
 - Standard: CS101HN, CS101MN, CS101SN
 - Low leak: CS101SL
- Small gate propagation delay
 - tpd = 12 ps (@1.2V, inverter, and F/O=1)
- Compiled memory macros (SRAMs and ROM)
- Application specific IPs
 - Computational cores: ARM, DSPs for communication and digital-AV
 - Mixed signals: ADCs and DACs
 - HSIF logics: PCI-Express
- High-speed interface SerDes macros (~10Gbps data rate)
- Standard I/Os: LVTTTL, SSTL, HSTL, LVDS, P-CML
- Wide supply voltage (0.80V to 1.30V for core)
- Various packages available (QFP, FBGA, EBGA, PBGA, FC-BGA)
- Design methodology and support
 - Methodology in place to support multi-million-gates hierarchical designs
 - Excellent design center support at Sunnyvale and Dallas
 - Worldwide service organizations for global support

90nm CMOS Standard Cell

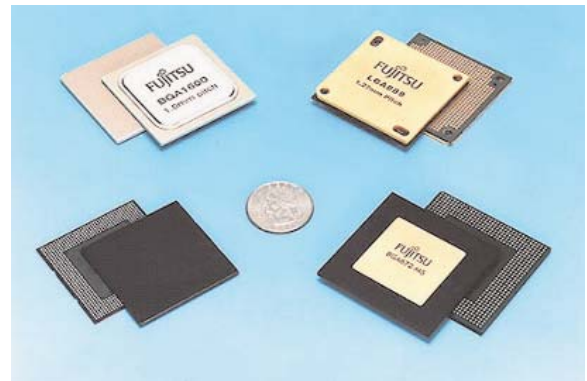
Description

CS101 Series, a group of 90nm standard cells, addresses the design challenges of the mobile device market in which low power consumption and multifunctionality are required. Also, the CS101 products serve the design needs of the leading-edge network devices, server applications and telecommunication equipment markets where high performance is vital.

This series consumes low power while realizing the performance and functions that are appropriate for user's applications. Furthermore, the design rules of this series conform to industrial standards, enabling the application of various commercial IPs.

Available Memory Macros

Memory Type	
1RW SRAM	(max. 576Kbits)
2RW SRAM	(max. 576Kbits)
ROM	(max. 4Mbits)



CS101 Maximum Ratings

Parameter	Symbol	Maximum Ratings	Unit	Note
Supply Voltage	VDDI	-0.5 to 1.8	V	For 1.2V internal logics
	VDDE	-0.5 to 3.6	V	For 2.5V external I/Os
Input Voltage	VI	-0.5 to VDDI+0.5	V	For 1.2V internal logics
		-0.5 to VDDE+0.5	V	For 2.5V external I/Os
Output Voltage	VO	-0.5 to VDDI+0.5	V	For 1.2V internal logics
		-0.5 to VDDE+0.5	V	For 2.5V external I/Os
Storage Temperature	Tstg	-55 to +125	degC	For plastic packages
Junction Temperature	Tj	-40 to +125	degC	

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 Printed in the U.S.A. WFS-FS-20164-9/2004