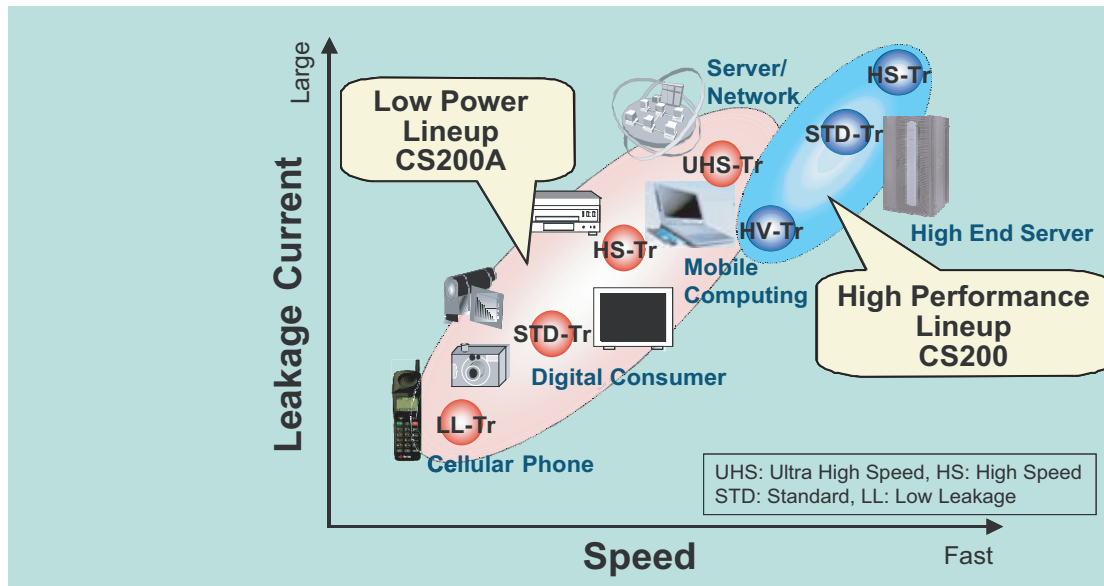


65nm CMOS Standard Cell

CS200 ASIC Series



► Features

- High integration
 - Transistor of 30–50nm gate length (ITRS road map 65nm)
 - 12-layer fine pitch, copper wiring, and low-K insulating material techniques
 - Maximum 180 million gates, nearly twice that of 90nm technology
 - 50% reduction in SRAM cell size
 - 30% increase in performance over 90nm
- Low power consumption/low leakage current
- I/O with pad structure with fine pad pitch technology for chip size reduction
- High-speed library and low-power library available
 - High speed: CS200HP
 - Low leak: CS200L
- Higher performance, gate propagation delay $t_{pd} = 4.4ps$ (@1.2V, inverter, and F/O = 1, CS200HP)
- Compiled memory macros: 1T and 6T SRAMs, and ROM
- Application specific IPs
 - Computational cores: ARM7, 9, 11, Communication and Digital-AV DSP
 - Mixed signals: Wide range of ADCs and DACs
 - HSIF logics: PCI-Express, XAUI, SATA, DDR, USB, HDMI
- High-speed interface SerDes macros (~10Gbps data rate)
- Wide range of PLLs: standard to high-speed 1.6GHz
- Standard I/Os: LVTTTL, SSTL, HSTL, LVDS, P-CML
- Wide supply voltage (0.80V to 1.30V for core)
- Triple V_{th} Transistor options
- Various packages available (QFP, FBGA, EBGA, PBGA, FC-BGA)
- Design methodology and support
 - Methodology in place to support multi-million-gates hierarchical designs
 - Excellent design center support at Sunnyvale and Dallas
 - Worldwide service organizations for global support

► Description

CS200 Series, 65nm standard cells CMOS process technology, addresses the design challenges of the PDA and mobile computing market in low power and multi-functionality. It also addresses the need of ultra high performance design in leading-edge

networking, server computing, and in complex telecom equipment applications. 65nm technology is available in 300mm fabrication and supports high volume wafer capacity in multiple manufacturing locations.

