

3-Channel DC/DC Converter IC

MB39A112

3-channel DC/DC converter IC with maximum oscillation frequency of 2.6MHz utilizing the pulse-width modulation method. Three channels are built into the TSSOP-20P package, enabling control and soft-start for each channel and making it an optimal built-in power supply for ADSL modems, etc.

Overview

The recent popularization of ADSL has been dramatic. Thus, FUJITSU has worked to develop built-in power-supply IC products for ADSL, etc. As a result, a 3-channel DC/DC converter IC, "MB39A112," which supports high-frequency operation, has been developed.

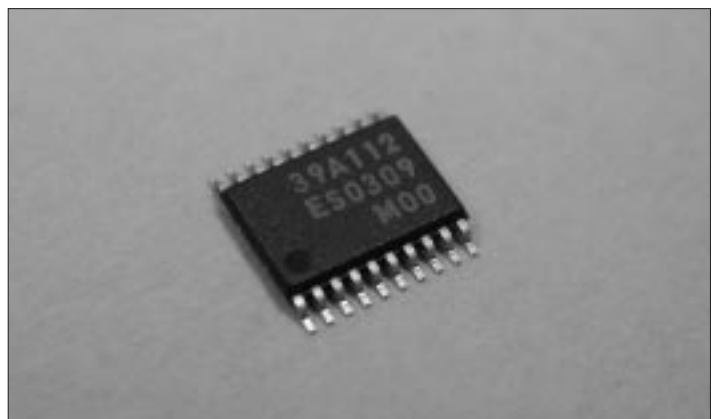
Together with the speedup in ADSL, there is a demand for built-in power supplies capable of fast switching. This product is a 3-channel DC/DC converter IC that uses the pulse-width modulation method (PWM type) to achieve a maximum oscillation frequency of 2.6MHz. It is optimal for down-conversion. Three channels are built into each TSSOP-20P package, and control or soft-start is possible for each channel. A constant-voltage bias circuit is incorporated into the output section to realize a high-frequency and high-efficiency DC/DC converter. Furthermore, in order to prevent an inrush current at power startup or an overcurrent at output short-circuit, a soft-start circuit and a timer-latch short-circuit detection circuit are included. This product is an optimal built-in power supply for ADSL modems, etc.

Features

- Supports the step-down method (CH1 to CH3)
- Power-supply voltage range: 7V to 25V

- Error amplifier threshold voltage:
1.0V \pm 1% (CH1), 1.23V \pm 1% (CH2, CH3)
- Oscillation frequency range: 250kHz to 2.6MHz
- Built-in soft-start circuit without load dependency
- Built-in timer-latch short-circuit protection circuit
- Built-in totem pole type output for Pch MOS FET
- Built-in constant-voltage bias circuit (VCCO-5V) for output section
- Package: TSSOP-20P

Photo 1 External View



Circuit configuration

Fig.1 shows the pin assignments, and **Fig.2** presents a block diagram.

This product consists of the following functional blocks.

DC/DC Converter Functions

■ Triangular Wave Oscillator Block

By connecting a capacitor and resistor with each of the CT and RT terminals for timing, a CT (amplitude 2.0V to 2.5V) triangular wave oscillation waveform is generated. The triangular wave oscillation waveform is input to the PWM comparator inside the IC.

■ Error Amplifier Block (Error Amp1 to Error Amp3)

An error amplifier detects the DC/DC converter's output voltage to output the PWM control signal. Since the optional loop gain can be established by connecting the output terminal of the error amplifier with the feedback resistor and capacitor of the inverted input terminal, stable phase compensation is provided for the system.

It is possible to prevent the inrush current at power startup by connecting a capacitor to the CS terminal of each channel. Performing soft-start detection at the error amplifier enables operation with a constant soft-start time that does not depend on the output load of the DC/DC converter.

■ PWM Comparator Block (PWM Comp.)

This is a voltage pulse-width modulator that controls the output duty according to the input/output voltage. It turns the output transistor on when the error amplifier output voltage is higher than the triangular wave voltage.

■ Output Block (Drive)

The output block adopts a totem pole type. It is capable of driving an external Pch MOS FET.

■ Bias Voltage Block (VH)

This block outputs VCCO-5V (typ.) as the minimum potential of the output circuit.

Table 1 ON/OFF Setup Conditions for Each Channel

CS1	CS2	CS3	Power	CH1	CH2	CH3
GND	GND	GND	ON	OFF	OFF	OFF
HiZ	GND	GND	ON	ON	OFF	OFF
GND	HiZ	GND	ON	OFF	ON	OFF
GND	GND	HiZ	ON	OFF	OFF	ON
HiZ	HiZ	HiZ	ON	ON	ON	ON

Channel Control Function

Each channel's ON/OFF is established by setting up the voltage for terminals CS1 to CS3.

Table 1 presents the ON/OFF setup conditions for the channels.

Protective Circuit Functions

■ Timer-Latch Short-Circuit Protection Circuit Block (SCP)

Each channel uses a short-circuit detection comparator (SCP Comp.) to constantly compare the output level from the error amplifier with the reference voltage.

If the DC/DC converter's load conditions are stable for all channels, output from the short-circuit detection comparator stays at level "L", maintaining the CSCP terminal at level "L". However, if the output voltage drops due to a sudden change in load conditions caused by a load short-circuit, etc., the SCP Comp. reaches level "H". Subsequently, charging is started for the short-circuit protection capacitor CSCP, which is externally attached to the CSCP terminal. The latch is set when the capacitor CSCP is charged to the threshold voltage (VTH≒0.72V) to turn the external FET (100% dead time) off. At this time, latch input is closed and the CSCP terminal is maintained at level "L". The latch for the timer-latch short-circuit protection circuit can be cancelled if the power supply (VCC) is terminated.

Figure 1 Pin Assignments

